Design and Implementation of Radio Frequency Power Feeding Networks for Antenna Array Applications

Simulation and Measurements of Multiport, Equal and Unequal, Fixed and Reconfigurable Radio Frequency Power Feeding Networks for Narrow and Ultra-Wideband Applications.

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Abstract

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Keywords: Wilkinson power divider, Uniplanar power divider, Multi-layer power divider, Multi-port power divider, Ultra-wideband power divider, Reconfigurable power divider, Equal and unequal power divider, Antenna array, Feeding network, Quarter-wavelength transformer.

Power dividers are vital components and widely used in radio technology, such as antenna arrays, power amplifiers, multiplexers and mixers. A good example is the well-known Wilkinson power divider with its distinctive feeding network characteristics. A comprehensive review indicated that limited research is carried out in the area of planar multiport and reconfigurable power dividers in terms of the power levels between output ports.

The main objectives of this work were to develop a small size power divider, a planer multi-output ports power divider and a power divider with a reconfigurable power division ratio. These power dividers were designed to operate over either an ultra-wideband frequency (3.1-10.6 GHz) or WLAN bands (2.4 or 5.2 GHz).

A novel multi-layered topology solved the complexity of interconnecting isolation resistors by introducing an additional layer below the ground layer. The prototype was fabricated and tested to validate the results. The measurements and simulation were in good agreement.

Finally, a novel uniplanar power divider with reconfigurable output power level difference was developed. The configurability feature was achieved by tuning the quarter wave transformer using one varactor diode. The power divider was applied to improve a full duplex system cancellation performance at the receiver element caused by interference from in-site transmitting antennas.

This study investigated fixed power dividers, multi-output power dividers and reconfigurable power dividers. The measurements validated by the simulation results and applications proved the designed power dividers could be used in practical applications.

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First and foremost, I would like to thank Allah, the Almighty, who gave me health, strength and the patience to complete my research. I would like to thank my father and mother, Dr Hussein Alwasity and Eng. Ibtisam Alwasity who did not forget me in their prayers, encouraged me, supported me in all possible ways including financially. Without their financial support, I would not be able to complete my journey. In addition, I would like to thank my beloved wife Ayat Alali beside my lovely son Jafar and sweet hard daughter Nowraa, for their support and patience in my stressful times. I would like to thank my brother and my sister Dr Hayder and Dr Duaa for their prayers and being there when needed.

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Acronyms

2D	Two Dimensional
3D	Three Dimensional
ADC	Analogue to Digital Converter
ADS	Advanced Designed System
AF	Array Factor
Balun	Balanced / Unbalanced
CST	Computer Simulation Technology
DGS	Defected Ground Structure
EBG	Electromagnetic Band Gap
FDD	Frequency Division Duplex
IEEE	Institute of Electrical and Electronics Engineers
ITU	International Telecommunication Union
LHCP	Left-Hand Circularly Polarised
LNA	Low Noise Amplifier
MIMO	Multiple Input Multiple Output
RHCP	Right-Hand Circularly Polarised
PSO	Particle Swarm Optimisation
PTFE	Poly Tetra Fluoro Ethylene
RF	Radio Frequency
SMA	Sub Miniature version A
SMD	Surface Mounted Device
TDD	Time Division Duplex
UWB	Ultra-Wide Band
VSWR	Voltage Standing Wave Ration
WLAN	Wireless Local Area Network

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Chapter 1

Thesis Introduction

1.1 Background

Power dividers are vital components in electromagnetic circuits, providing matched three port transmission lines where each line has a length of a quarter of a wavelength at the designed centre frequency. The original concept was introduced in 1960 by E.J. Wilkinson [1]. He introduced a resistor between the output ports and improved the return loss and output ports isolation of the conventional T-junction power divider. However, this design gave a narrow operational bandwidth. Some later studies have developed methods to increase the feasible bandwidth such as adding extra sections [2], introducing stubs to sections [3-6], and using a defected ground plane [7]. Commercial ultra-wideband (UWB) system applications, such as antenna arrays, are increasingly developing and demanding that the power divider should satisfy bandwidth requirements while providing a high level of isolation between output ports, and a constant insertion loss [8].

Wilkinson power dividers are not easy to implement as a planar structure for layouts with more than two output ports since the isolation resistors need to be connected in a star configuration and thus they require crossovers. That makes it difficult to implement single stage planar structures. A lot of studies have been reported methods to overcome this problem. The common method is by implementing several cascaded stages [9] but few of them have been successful

in implementing planar structures [10]. However, power dividers with cascaded stage structures will suffer from additional conductor losses due to additional transmission line lengths and sometimes amplitude imbalance.

Some applications require reconfigurable power dividers such as antenna array feeding networks for beamforming [11], diversity applications to obtain a better signal to noise ratio [12] and power amplifier feeds designed to improve efficiency [13]. Wilkinson power dividers with unequal division ratio split the input power by using two asymmetric quarter wave transformers [2]. In applications where a high power division ratio is required, one of the quarter wave transformers may have high characteristic impedance, i.e. it becomes a narrower transmission line, which is more difficult to implement accurately due to fabrication tolerance. Such a line also suffers from low power handling capacity. Several techniques have been introduced to overcome that problem such as a defected ground structure microstrip line [14-18], using a coplanar waveguide with electromagnetic bandgap [19, 20], offsetting a double-sided parallel strip line [21], increasing the distance of the offset or by decreasing the strip line width that makes the power handling worse. Also, applying a groove alongside a microstrip line can be used to increase a microstrip line impedance [22]. The last technique needs an additional fabrication process to properly applying the groove accurately.

1.2 Aims and Objectives

The aim of this research is to investigate and contribute to the RF feeding network for antenna array applications to get a better understanding and to enhance various feeding networks. The aspects investigated in this research included

ultra-wideband, multi-output ports and reconfigurable power dividers for microwave applications.

Objectives identified to achieve these aims were to:

1. Conduct a comprehensive study of the major techniques of Wilkinson power divider feeding and manifestations for fixed and reconfigurable feeding networks.
2. Perform an analytical study of Wilkinson power dividers to find a solution to feeding network limitations.
3. Fully modelling different Wilkinson power dividers using CST Microwave studio software.
4. Conduct experimental measurements and validate results with simulation.

The major contributions of this work are:

1. A UWB Wilkinson power divider is presented in section 3.1. The modified model is compared to other UWB power divider models using simulation data and measurements. Different structures are considered to achieve a miniature design. It is found that the proposed structure is better in performance and smaller in size compared to other published works.
2. A novel design for microstrip-fed multi-output ports planar Wilkinson power divider is proposed, designed and fabricated in section 3.2. The proposed power divider operates in a wideband frequency range with a low insertion loss imbalance. The power divider adopts a three -

layered structure and microstrip feeding technique solving isolation resistor interconnection crossover problem for dividers having more than two output ports. Two different permittivity substrates were selected to simplify the design structure.

3. A novel reconfigurable Wilkinson power divider with an equal split to 8 dB power difference between output ports is presented in section 3.3. The proposed power divider adopts the microstrip coupled line technique to implement a high impedance quarter wave transformer section with unequal output power values. A varactor diode is placed between the coupled line to achieve the reconfigurability feature.
4. A full-duplex communication system is presented in section 5.4 in which antenna cancellation techniques are studied that can be used to achieve the self-interference cancellation. The full duplex system consists of three monopole antennas, two of them as transmit antennas and the other as a receive antenna. In addition, the performance of the system is tested by measurements.

1.3 Organization of the Thesis

Chapter 2: This chapter provides a comprehensive study of different power dividers and antennas. The first part focuses on understanding the basic concepts and analysing Wilkinson power dividers using even-odd mode analysis. In addition, it provides an insight into multi-output ports and unequal power dividers. The second part explores many antenna types and focuses on understanding their properties.

Chapter 3: This chapter opens with a historical review of the Wilkinson power divider. Different structures for UWB power dividers are studied, designed and implemented. In addition, a novel multi-output ports power divider and its design procedure is presented in the second section of this chapter. The last section presents a novel reconfigurable power divider.

Chapter 4: This chapter presents three different antenna types, which have been simulated and fabricated. The conducted measurement showed good agreement with simulation. The first antenna is a coaxial fed rectangular patch antenna designed to resonate at 5.2 GHz. The second antenna is a microstrip-fed Yagi-Uda antenna designed to support the 2.4 GHz WLAN applications. The third antenna is a microstrip-fed dual-band antenna designed to support both 2.4 and 5.2 GHz WLAN applications. A brief description and design equation are included for each antenna.

Chapter 5: A practical application is presented in chapter five for each power divider designed in chapter three. This chapter is divided into four sections. The first section presents an application using the rectangular patch antenna array with embedded feeding network. The second section presents an antenna array consisting of four Yagi-Uda antennas benefiting from the multi-output ports power divider as a feeding network. The third section presents a dual-band antenna array as an application for the UWB power divider. The last section presented a simple full duplex communication system using self-interference cancellation technique achieved by using the reconfigurable power divider designed in chapter three.

Chapter 6: This chapter gives the conclusion for the whole thesis and provides the outcomes of this work. In addition, suggestions for future work that can extend the archived results are presented in this chapter.

1.4 List of Publications

1. **A. H. Ali**, K. W. Hameed, N. T. Ali, M. S. Bakr, R. Asif, R. A. Abd-Alhameed, et al., "Reconfigurable Wilkinson power divider with unity to 8 dB output power differences using one varactor diode," presented in the Antennas & Propagation Conference (LAPC), Loughborough, 2018.
2. **A. H. Ali**, K. W. Hameed, N. T. Ali, M. S. Bakr, R. A. Abd-Alhameed, and N. J. McEwan, "A general design for multi-output ports planar Wilkinson power divider," Microwave and Optical Letters, under the press, 2018.
3. M. Alibakhshikenari, B. Virdee, C. H. See, R. Abd-Alhameed, **A. H. Ali**, F. Falcone, Ernesto Limiti, "Study on Isolation Improvement Between Closely Packed Patch Antenna Arrays Based on Fractal Metamaterial Electromagnetic Bandgap Structures," Microwaves, Antennas & Propagation, IET, 2018.
4. Chemseddine Zebiri, Djamel Sayad, Fatiha Ben Abdelaziz, Mohamed Lashab, and **Ammar Ali**. A chapter in the book titled, Antenna Fundamentals for Legacy Mobile Applications and beyond. Chapter title, Impact of Microstrip-Line Defected Ground Plane on Aperture-Coupled Asymmetric DRA for Ultra-Wideband Applications. Springer, 2018.
5. A. Jasim, K. Younus, **A. Ali**, K. Sayidmarie, A. Alhaddad, and R. Abd-Alhameed, "A simple self-interference cancellation technique for full

duplex communication," in Internet Technologies and Applications (ITA), 2017, 2017, pp. 224-229.

6. I. M. Danjuma, F. M. Abdussalam, **A. Ali**, R. A. Abd-Alhameed, and J. N. Noras, "Reconfigurable Design Model of Bow-Tie Dipole Adjacent Lossy Dielectric Using Optimisation Method in Hybrid Electromagnetic Technology," URSI Conference, Manchester University, Paper No. 9, 2016.
7. **A. H. Ali**, R. A. Abd-Alhameed, J. M. Noras, and M. B. Child, "An ultrawideband power divider for antenna array feeding network," in Antennas & Propagation Conference (LAPC), 2016 Loughborough, 2016, pp. 1-4.
8. **A. H. Ali**, R. A. Abd-Alhameed, Y. F. Hu, C. Kyriacou, and M. B. Child, "A Design Procedure for a 1-to-4 Ultra-Wideband Wilkinson Power Divider," Broadband: Journal of the SCTE, vol. 38, 2016.
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11. Karam Younus, Roger Clarke, Raed Abdulhameed, **Ammar Ali** et al., "A novel beam steering design for phased array antennas " URSI Conference, Manchester University, Paper No. 19, 2015.

12. **A. Ali** and R. A. Abd-Alhameed, "Miniature 1 to 2 ultra-wideband power divider," URSI Conference, Manchester University, Paper No. 7, 2015.
13. M. Akinsolu, **A. Ali**, A. Atojok, E. Ibrahim, I. Elfergani, R. Abd-Alhameed, et al., "Novel Quadrifilar Helical Antenna for RFID Applications Using Genetic Algorithms," Session 1P0, p. 585, 2015.
14. **A. Ali**, A. Atojok, E. Ibrahim, R. A. Abd-Alhameed, P. S. Excell, F. Elmegri, et al., "Design and optimisation of quadrifilar helical antenna for RFID applications using genetic algorithms " URSI Conference, Manchester University, Paper No. 9, 2014.

Chapter 2

Literature Review

2.1 Power Dividers Fundamentals

Power dividers are passive components used in many microwave and RF circuits for power dividing or power combining. In the power division mode, an input signal is divided into two or more output signals, while a power combiner accepts two or more input signals and combines them. The divider may have three or more ports and ideally considered lossless. Power dividers with two output ports can generally be classified into two types. According to the output power division ratio as equal power dividers or known as 3 dB power dividers and unequal power divider that provide output signals with an unequal magnitude depending on the division ratio. The second calcification for power divider is according to the output power phase difference as in phase and out of phase power dividers.

Power dividers are typically considered as three port networks. The scattering parameter matrix (S-matrix) of an arbitrary three-port network has nine independent elements:

$$[S]=\begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{2.1}$$

The device must be reciprocal and its S-matrix will be symmetric ($S_{ij} = S_{ji}$) if it is passive and contains no anisotropic materials. Usually, to avoid power loss, a

junction that is lossless and matched at all ports is preferable. It is impossible to construct such a three-port lossless reciprocal network that is matched at all ports.

If all ports are matched, then S_{ii} is equal zero, and if the network is reciprocal, then the S-matrix of (2.1) is reduced to:

$$[S]=\begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{12} & 0 & S_{23} \\ S_{13} & S_{23} & 0 \end{bmatrix} \tag{2.2}$$

If the network is also lossless, then the following conditions apply:

$$|S_{12}|^2+|S_{13}|^2=1 \tag{2.3}$$

$$|S_{12}|^2+|S_{23}|^2=1 \tag{2.4}$$

$$|S_{13}|^2+|S_{23}|^2=1 \tag{2.5}$$

$$S_{12}^{*}S_{23}=0 \tag{2.6}$$

$$S_{23}^{*}S_{12}=0 \tag{2.7}$$

$$S_{12}^{*}S_{13} = 0 \tag{2.8}$$

Equations (2.6) to (2.8) are showing that at least two of the three parameters S_{12}, S_{13} or S_{23} must be zero. However, this condition will be always inconsistent with one of the equations (2.3) to (2.5), implying that a three-port network cannot be simultaneously lossless, reciprocal and matched at all ports. If anyone of these three conditions is relaxed, then a physically realizable device is possible [2].

Alternatively, a lossless and reciprocal three-port network can be physically realized if only two of its ports are matched. If ports one and two are the matched ports, then the S-matrix is written as:

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{12} & 0 & S_{23} \\ S_{13} & S_{23} & S_{33} \end{bmatrix} \tag{2.9}$$

To be lossless, the following conditions must be satisfied:

$$S_{13}^{*}S_{23} = 0 \tag{2.10}$$

$$S_{12}^{*}S_{13} + S_{23}^{*}S_{33} = 0 \tag{2.11}$$

$$S_{23}^{*}S_{12} + S_{33}^{*}S_{13} = 0 \tag{2.12}$$

$$|S_{12}|^2 + |S_{13}|^2 = 1 \tag{2.13}$$

$$|S_{12}|^2 + |S_{23}|^2 = 1 \tag{2.14}$$

$$|S_{13}|^2 + |S_{23}|^2 + |S_{33}|^2 = 1 \tag{2.15}$$

Equations (2.13) and (2.14) show that $|S_{13}| = |S_{23}|$, so equation (2.10) leads to the result that $S_{13} = S_{23} = 0$. Then, $|S_{12}| = |S_{33}| = 1$.

2.1.1 T-Junction Power Divider

The T-junction power divider can be implemented in virtually any type of transmission line medium. It is considered a simple three-port network that can be used for power combining or power division. The conventional T-junction power divider is lossless but suffers from the issue of not being matched at all ports. Moreover, there is no isolation between output ports.

A junction of three transmission lines can model the lossless T-junction divider, as shown in Figure 2.1 [2]. In general, there may be fringing fields and higher order modes associated with the discontinuity at such a junction, leading to stored energy that can be accounted for by a lumped susceptance that is denoted by B in the following equation. In order for the divider to be matched to the input line of a characteristic impedance of Z_0, the admittance can be written as:

$$Y_{in} = jB + \frac{1}{Z_1} + \frac{1}{Z_2} = \frac{1}{Z_0} \tag{2.16}$$

The characteristic impedances are real if the transmission lines are assumed to be lossless or of a low loss, then equation (2.16) can be reduced to the following equation if assuming B = 0:

$$\frac{1}{Z_1} + \frac{1}{Z_2} = \frac{1}{Z_0} \tag{2.17}$$

In practice, if B is not negligible, some type of discontinuity compensation or a reactive tuning element can be usually used to cancel this susceptance, at least over a narrow frequency range.

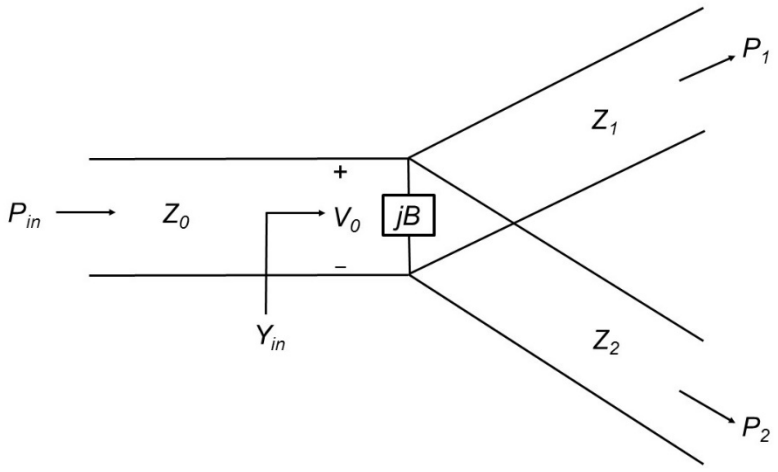


Figure 2.1. Transmission line model of a lossless T-junction power divider.

Various power division ratios can be provided by selecting different impedances for the output ports (Z_1 and Z_2). Thus, an equal split (known as 3 dB power

divider), can be made by using two 100 Ω output lines to have a 50 Ω input line. To bring the impedance of the output lines back to the desired levels, quarter-wave transformers can be used. The input line will be matched when the output lines are matched. However, there will be a mismatch looking into the output ports and there will be no isolation between them.

To find the output characteristic impedances for a lossless T-junction power divider so that the output powers ratio is 2:1 and a source impedance of 50 Ω, the power at the input port needs to be found.

$$P_{in} = \frac{1}{2}\frac{V_0^2}{Z_0}$$

and

$$P_1 = \frac{1}{2}\frac{V_0^2}{Z_1} = \frac{1}{3}P_{in}$$

$$P_2 = \frac{1}{2}\frac{V_0^2}{Z_2} = \frac{2}{3}P_{in}$$

so the characteristic impedance for output ports is:

$$Z_1 = 3Z_0 = 150\Omega$$

and

$$Z_2 = \frac{3}{2} Z_0 = 75\Omega$$

so

$$Z_{in} = \frac{75 * 150}{75 + 150} = 50\Omega$$

Concluding from that the input impedance is matched to the 50 Ω source impedance.

An impedance of 30 Ω can be seen (50 Ω in parallel to 75 Ω) when looking into the 150 Ω output line, while a 37.5 Ω can be seen when looking into the 75 Ω output line (50 Ω in parallel to 150 Ω). Looking into these ports, the reflection coefficients are seen as:

$\Gamma_1 = \frac{30 - 150}{30 + 150} = -0.666$ that is equivalent to -3.52 dB.

$\Gamma_2 = \frac{37.5 - 150}{37.5 + 150} = -0.6$ that is equivalent to -4.44dB.

If a three-port power divider contains lossy components, it can be made to be matched at all ports, although the two output ports may not be isolated [23]. The circuit for such divider is illustrated using lumped-element resistors in Figure 2.2 [2]. An equal-split divider is shown, but unequal power division ratios are also possible.

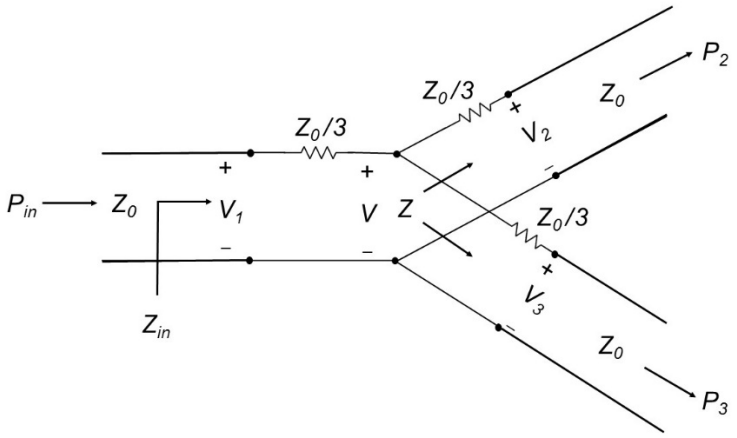


Figure 2.2. An equal split three-port resistive power divider.

The resistive divider of Figure 2.2 can be easily analysed using circuit theory. Assuming that all ports are terminated in the characteristic impedance Z_0, the impedance Z, seen looking into the $Z_0/3$ resistor followed by a terminated output line, is:

$$Z = \frac{Z_0}{3} + Z_0 = \frac{4Z_0}{3} \tag{2.18}$$

then the input impedance of the divider is:

$$Z_{in} = \frac{Z_0}{3} + \frac{2Z_0}{3} = Z_0 \tag{2.19}$$

This shows that the input is matched to the feeding line. The output ports are also matched because of the network is symmetric from all three ports. Thus:

$$S_{11} = S_{22} = S_{33} = 0 \tag{2.20}$$

If the voltage at port one is V_1, then by using the voltage division, the voltage V at the centre of the junction is:

$$V = V_1 \frac{2Z_0 / 3}{Z_0 / 3 + 2Z_0 / 3} = \frac{2}{3} V_1 \tag{2.21}$$

and the output voltages are, again found by the voltage division:

$$V_2 = V_3 = V \frac{Z_0}{Z_0 + Z_0 / 3} = \frac{3}{4} V = \frac{1}{2} V_1 \tag{2.22}$$

Thus, $S_{21} = S_{31} = S_{23} = 1/2$, so the output powers are 6 dB below the input power level. The network is reciprocal, so the S-matrix is symmetric, and it can be written as:

$$[S] = \frac{1}{2} \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \tag{2.23}$$

The power delivered to the input of the divider is:

$$P_{in} = \frac{1}{2} \frac{V_1^2}{Z_0} \tag{2.24}$$

While half of the supplied power is dissipated in the resistors as the output power can be calculated as shown:

$$P_2 = P_3 = \frac{1}{2}\frac{(1/2V_1)^2}{Z_0} = \frac{1}{8}\frac{V_1^2}{Z_0} = \frac{1}{4}P_{in} \tag{2.25}$$

2.1.2 Wilkinson Power Divider

The lossless T-junction power divider suffers from the disadvantage of not being matched at all ports, and it does not have isolation between output ports. The resistive divider can be matched at all ports, but even though it is not lossless, isolation is still not achieved. A lossy three-port network can be made having all ports matched, with isolation between output ports. The Wilkinson power divider is such a network, with the useful property of appearing lossless when the output ports are matched; that is, only reflected power from the output ports is dissipated [2].

The Wilkinson power divider can be made with arbitrary power division, but the equal-split will be considered first. This divider is often made in a microstrip line form and this type of transmission line will be considered in this thesis.

The corresponding transmission line circuit for equal split and equal phase power divider is shown in Figure 2.3 [2]. This circuit can be analysed by reducing it to two simpler circuits driven by symmetric and antisymmetric sources at the output ports. For simplicity, all impedances can be normalised to the characteristic

impedance Z_0, and the circuit is redrawn as shown in Figure 2.4 [2], with voltage generators at the output ports.

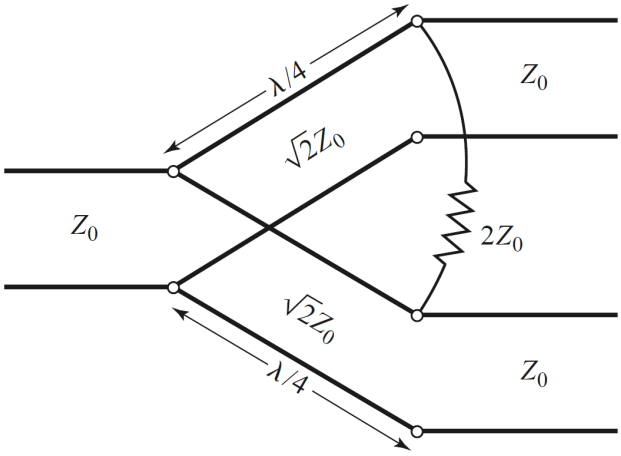


Figure 2.3. The equivalent transmission line circuit for the equal-split and phase Wilkinson power divider.

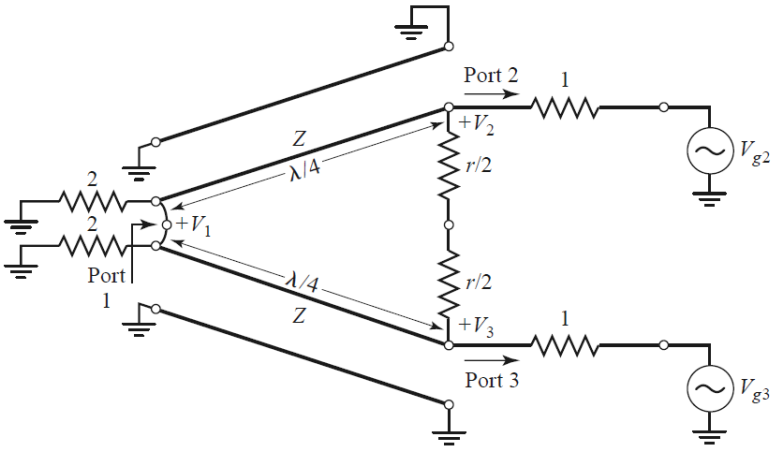


Figure 2.4. The normalized and symmetric form of the equal-split and phase Wilkinson power divider.

The three-port network is symmetric across the middle plane. The two input port resistors of a normalized value of two are combined in parallel to generate one normalized resistor of a normalized value of one that represents the matched

source impedance. The λ/4 transmission line shows a normalised characteristic impedance Z, and the isolation resistor has a normalised value of r. For equal splitting power divider the following conditions should be achieved:

$$Z = \sqrt{2}Z_0 \tag{2.26}$$

and

$$r = 2Z_0 \tag{2.27}$$

The S-matrix for the Wilkinson power divider can be found using even-odd mode analysis that uses circuit symmetry and superposition. For the even mode analysis, the output ports excitation considered to be equal and their value is $2V_0$, so there is no current flows through the r/2 resistors. Besides that, there is no current flows through the short circuit between the inputs of the two λ/4 transformer lines at port one. According to that, the equivalent circuit in Figure 2.4 is simplified into bisection as shown in Figure 2.5 [2] with open circuits. The ground side of the circuit is not shown to simplify the diagram.

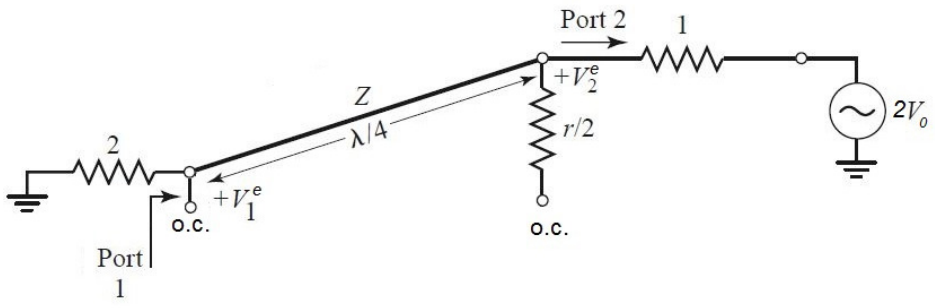


Figure 2.5. Bisection of the normalized and symmetric form circuit of the equal-split and phase Wilkinson power divider for even mode excitation.

Looking into port two, the impedance is:

$$Z_{in}^{e} = \frac{Z^2}{2} \tag{2.28}$$

The transmission line works as a λ/4 transformer. So, if Z=$\sqrt{2}$, port two will be matched for even mode excitation, and then, $V_2^e = V_0$ since $Z_{in}^e = 1$. The r/2 resistor can be neglected as its other end is open circuited in the even mode. If x=0 at port one and x=- λ/4 at port 2, the voltage on the transmission line can be written as:

$$V(x) = V^{+}(e^{-j\beta x} + \Gamma e^{j\beta x}) \tag{2.29}$$

then

$$V_1^e = V(0) = V^{+}(1+\Gamma) = jV_0\frac{\Gamma - 1}{\Gamma + 1} \tag{2.30}$$

and

$$V_2^e = V(-\lambda/4) = jV^{+}(1-\Gamma) = V_0 \tag{2.31}$$

The reflection coefficient Γ is that seen at port one, looking at the resistor of normalised value $2Z_0$, so:

$$\Gamma = \frac{2-\sqrt{2}}{2+\sqrt{2}} \tag{2.32}$$

thus

$$V_1^e = -jV_0\sqrt{2} \tag{2.33}$$

For the odd mode excitation, the voltage generator of port two is equal $2V_0$, which is equal to the negative value of the voltage generator of port three. That produces a voltage null along the middle of the equivalent circuit in Figure 2.4. The bisection circuit of Figure 2.4 is shown in Figure 2.6 [2] for the odd mode analysis, by grounding the network at two points on its middle plane.

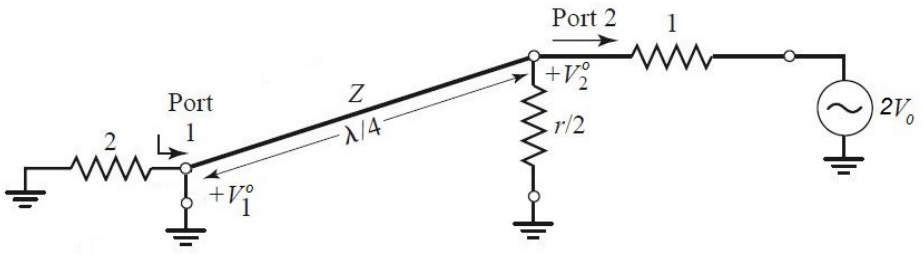


Figure 2.6. Bisection of the normalized and symmetric form circuit of the equal-split and phase Wilkinson power divider for odd mode excitation.

Looking into port two, there is an impedance of r/2 in parallel with the λ/4 long transmission line that is shorted at port one, and it seems an open circuit at port two. That means port two is matched in the odd mode excitation if r equals two. Thus $V_2^o = V_0$ and $V_1^o = 0$, which means all of the power is transmitted to the r/2 resistors and none is going to port one.

To find the input impedance at port one, Figure 2.7 [2] is used that illustrates an equivalent circuit of Wilkinson power divider when port one and three are terminated to matched loads. It is similar to an even mode excitation since the value of the voltage generators at the output ports are equal. There is no current flowing through the resistor of the normalized value of two, and it could be removed. The simplified circuit is shown in Figure 2.8 [2]. The two parallel λ/4 transformers are terminated in normalised loads, and the impedance is calculated by:

$$Z_{in} = \frac{1}{2}(\sqrt{2})^2 = 1 \tag{2.34}$$

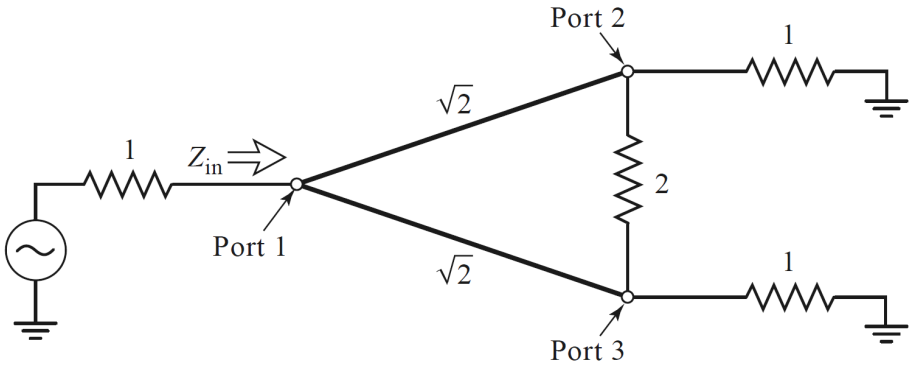


Figure 2.7. Terminated output ports Wilkinson power divider.

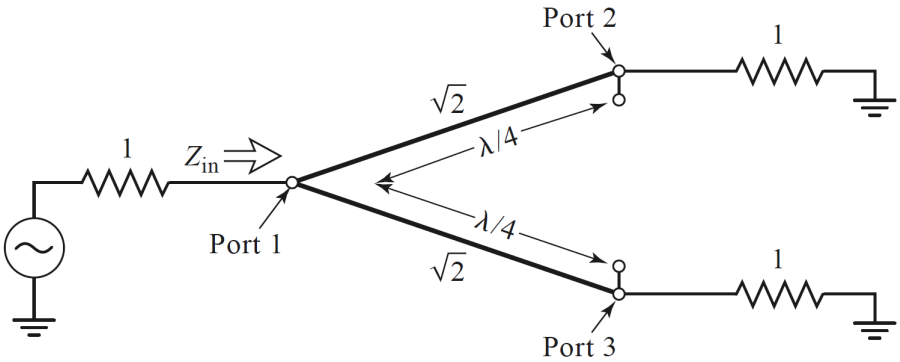


Figure 2.8. Bisection of the terminated output ports Wilkinson power divider.

From the above analysis, the S-parameters can be summarised as:

$S_{11} = 0$ (Z_{in}=0 at port 1)

$S_{22} = S_{33} = 0$ (matched output ports for even and odd modes)

$S_{21} = S_{12} = \frac{V_1^e + V_1^o}{V_2^e + V_2^o} = -\frac{j}{\sqrt{2}}$ (symmetry due to reciprocity)

$S_{31} = S_{13} = -\frac{j}{\sqrt{2}}$ (symmetry of output ports)

$S_{23} = S_{32} = 0$ (due to short or open at bisection)

Therefore, the S-matrix is written as:

$$[S] = \begin{bmatrix} 0 & -j/\sqrt{2} & -j/\sqrt{2} \\ -j/\sqrt{2} & 0 & 0 \\ -j/\sqrt{2} & 0 & 0 \end{bmatrix} \quad (2.35)$$

It can be seen from the above equations that all ports are matched when the divider is terminated with matched loads. Besides that, it can be seen that no power is dissipated in the resistor when the network is driven at port one and the

outputs are matched. Therefore, the Wilkinson power divider is lossless when the output ports are matched. The reflected power at port two and three is lost in the resistor. There is a high isolation between port two and port three because S_{23} = S_{32}= 0.

The Wilkinson power divider can be also generalized to an N-way output divider or combiner [1] as shown in Figure 2.9.

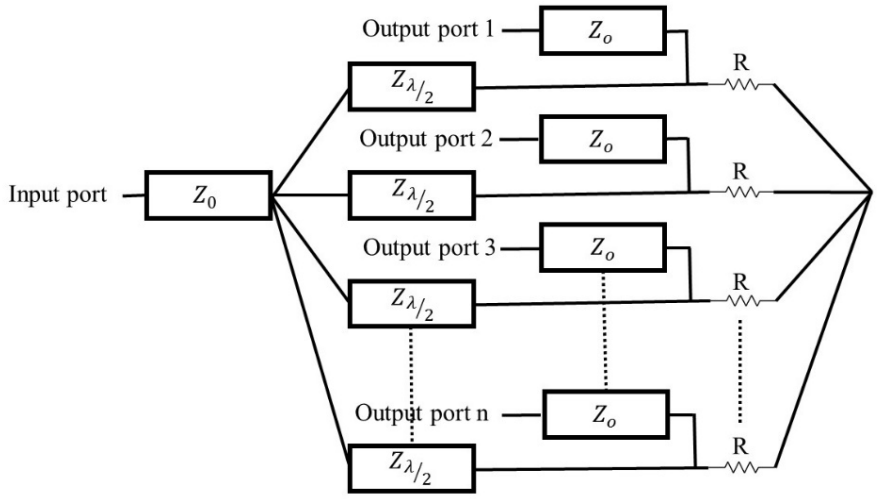


Figure 2.9. An N-way Wilkinson power divider diagram.

This circuit can be matched at all ports with high isolation between output ports. However, the disadvantage is that the divider requires crossovers for the isolation resistors when N is more than three, which makes the fabrication difficult in a planer form [2].

$$Z_{\lambda/2} = \sqrt{N} Z_0 \tag{2.36}$$

$$R = Z_0 \tag{2.37}$$

Wilkinson power dividers can be also designed as an unequal power splitter, in which one of the quarter wave transformers has higher impedance compared to the other one. Figure 2.10 [2] shows a circuit diagram for unequal split Wilkinson power divider. If the power division ration between output ports is:

$$K^2 = \frac{P_3}{P_2} \tag{2.38}$$

then the following equation applies:

$$Z_{03} = Z_0 \sqrt{\frac{1+K^2}{K^3}} \tag{2.39}$$

$$Z_{02} = K^2 Z_{03} = Z_0 \sqrt{K(1+K^2)} \tag{2.40}$$

$$R = Z_0 \left(\frac{K^2+1}{K} \right) \tag{2.41}$$

$$R_3 = Z_0 / K \tag{2.42}$$

$$R_2 = Z_0 K \tag{2.43}$$

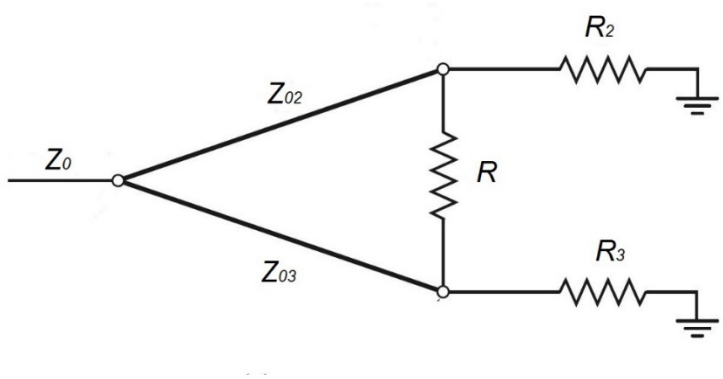


Figure 2.10. Unequal split Wilkinson power divider circuit diagram.

Equations (2.36) to equation (2.41) also can be applied for the equal split Wilkinson power divider by considering K^2 equals one. In addition, it is noted that the output ports are connected to R_2 and R_3 instead of connecting it to Z_0 in the equal split Wilkinson power divider and their value equals 50 Ω in the equal split Wilkinson power divider design.

2.2 Antenna Fundamentals

Antennas are devices for radiating or receiving radio waves. They are an essential transitional structure between transmission line (guiding device) and free-space. The antenna could take to operation forms, one transmitting electromagnetic energy from the source to space which is known as a transmitter antenna, or from the space to the receiver, which is known as a receiver antenna. The antenna radiation pattern is used to describe the electromagnetic radiation distribution and it is achieved by studying the current flow on the antenna. Figure 2.11 [24] shows the antenna operating as a transition device.

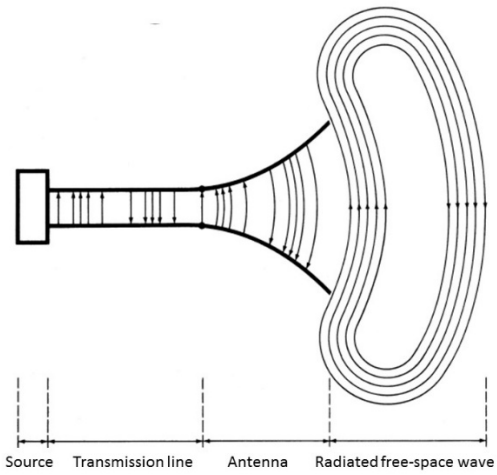


Figure 2.11. Antenna as a transition device.

There are many types of antenna configuration; Figure 2.12 illustrates some wire antenna configurations. There are many shapes of wire antennas such as a straight wire, loop antenna and helical antenna. Loop antennas may take several forms such as circular, ellipse, rectangular and any other shapes, but the circular loop is the most commonly used one because it is simple to construct.

Figure 2.12. Wire antenna configurations: dipole and loop antennas.

Figure 2.13 shows different types of patch antennas such as a rectangular microstrip-fed antenna and a coaxial-fed circular patch antenna. They are commonly used antennas because it eases to analyse, easy to fabricate and have attractive radiation characteristics, especially low cross-polarization radiation. Besides that, microstrip antennas are low profile, convenient for planar and nonplanar surfaces, simple and inexpensive to fabricate.

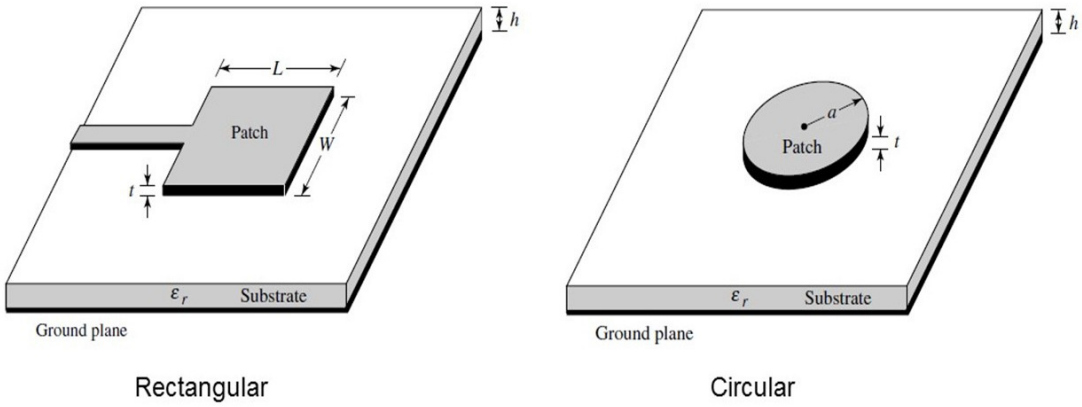


Figure 2.13. Rectangular and circular patch antennas.

An ideal antenna is one which will radiate all the delivered power from the transmitter to a certain desired direction or several directions. In practice, such an ideal antenna is not available but very high-performance antennas may be closely approachable. Various types of antenna are available, which have not been discussed that have different forms in order to achieve the desired characteristics for the particular application. The equivalent circuit for a transmitting antenna is shown in Figure 2.14 [24].

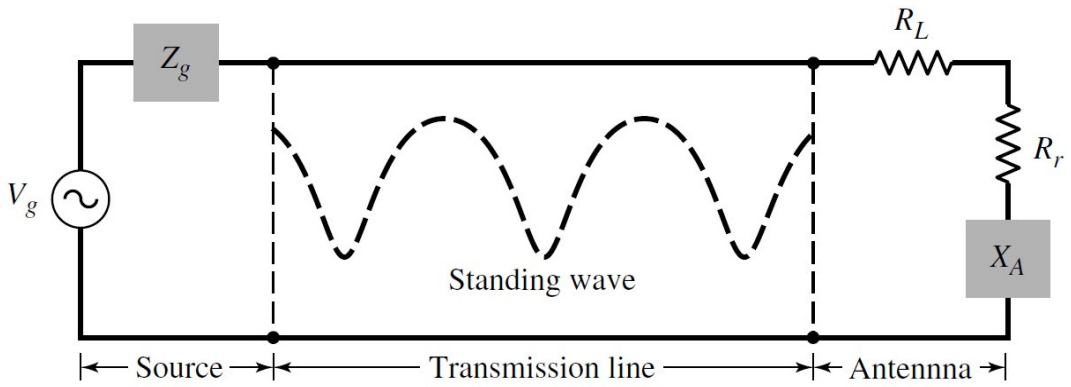


Figure 2.14. The equivalent circuit for a transmitting antenna.

The source considered an ideal signal generator, the transmission line has a characteristic impedance of Z_C. Antenna impedance Z_A is given by the following equations:

$$Z_A = R_A + jX_A \tag{2.44}$$

$$R_A = R_L + R_r \tag{2.45}$$

Where, R_A is the antenna resistance and R_L is the load resistance, which includes dielectric loss and conduction loss, while R_r stands for radiation resistance and X_A is antenna reactance.

By matching antenna impedance Z_A and transmission line characteristic impedance Z_C, the standing wave is decreased, and the energy storage capacity of the transmission line is minimised. A maximum power is delivered to the antenna from the source as a result of that.

This condition is calculated by conjugate matching:

$$R_g = R_A = R_L + R_r \tag{2.46}$$

$$X_g = -X_A \tag{2.47}$$

In these equations, R_g is the source resistance, X_g represents source reactance and X_A represents antenna reactance. The power reflected from the antenna towards the source, as shown in Figure 2.14 is known as S-parameter. The S-parameter shows the relationship between input power and output power for the antenna with respect to frequency. The S-parameter or S_{11} is also known as the reflection coefficient, which represents the reflected power from the antenna [24].

2.2.1 Radiation Pattern

According to IEEE standards, the radiation pattern is defined as “the spatial distribution of a quantity that characterizes the electromagnetic field generated by an antenna” [25]. The radiation pattern can be represented either graphically or mathematically. Generally, there are three types of antenna radiation patterns: isotropic, directional and omnidirectional. Practically, an isotropic radiation pattern antenna cannot be created; theoretically, it is considered as lossless antenna and it has equal radiation intensity in all spherical directions. An antenna that receives or radiates electromagnetic waves in a certain direction more than in other directions is known as a directional antenna. The radiation pattern is shown by lobes, which can be classified into main and side lobes. The lobe that contains the strongest radiation intensity is known as the main lobe and also known as a major lobe, while the rest are known as minor lobes. The main lobe half power beamwidth is the angular separation between half-power points that are also known as 3 dB points. Minor lobes can be classified into side lobes and back lobe as shown in Figure 2.15 [24]. The back lobe refers to a minor lobe, which is in the opposite direction of the main lobe. Minor lobes show radiation towards undesired directions that should be minimised in antenna designs. Minor

lobe levels (side lobe or back lobe ratio) are used for expressing the ratio of the power density between the minor lobes and the main lobe. Low minor lobe level is a very important feature in antenna array designs. Finally, the omnidirectional radiation pattern is a special case of a directional pattern, that generates, a non-directional pattern, in a given plane and a directional pattern in any orthogonal plane [24].

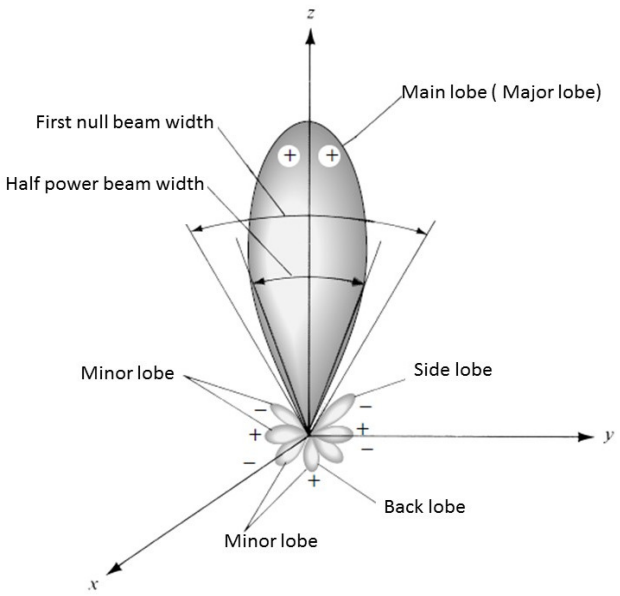


Figure 2.15. Directional antenna radiation pattern.

2.2.2 Field Regions

The antenna radiation area is divided into three regions. The first one is a reactive near-field region while the second one is a radiating near field or known as Fresnel region and the third one is a far-field or known as Fraunhofer region. All regions are shown in Figure 2.16 [24]. There are different preferences among the three regions. The reactive near-field region is the area immediately surrounding the antenna and the distance is determined by:

$$R_1 = \sqrt{\frac{D^3}{\lambda}} \tag{2.48}$$

Where D is the largest antenna dimension and λ stands for the wavelength. The radiating near-field region is the portion between the reactive near-field region and the far-field region, wherein the angular field distribution varies according to the distance from the antenna [24]. The inner boundary space is calculated by:

$$R_2 \geq 0.62\sqrt{D^3/\lambda} \tag{2.49}$$

and the outer boundary is the distance calculated by:

$$R_2 < 2D^2/\lambda \tag{2.50}$$

The far-field region is the antenna radiation space where the angular field distribution is completely independent of the radial distance from the antenna. The distance is estimated by:

$$R_2 \geq 2D^2/\lambda \tag{2.51}$$

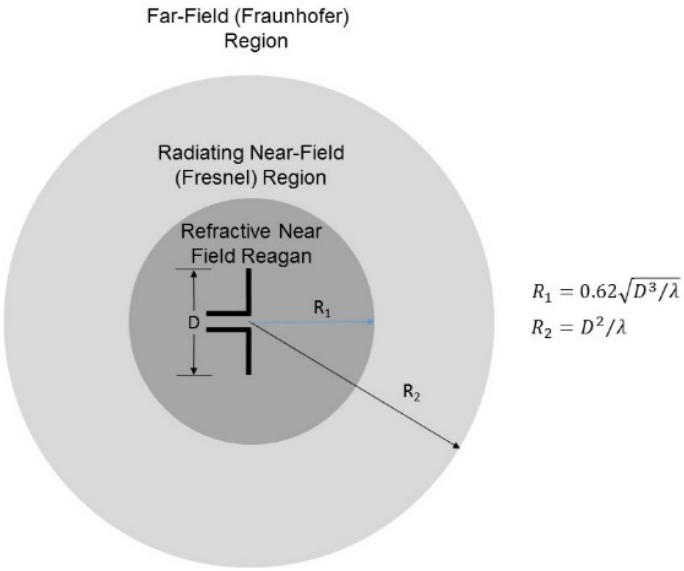


Figure 2.16. Field regions of an antenna.

2.2.3 Radiation Power Density

The average power radiated by an antenna in a particular direction is defined as the radiation power density, P_r (W/m^2). The following equation describes the relationship between power density and field intensities [24].

$$P_r(r,\theta,\phi) = \frac{1}{2}\left[E \times H^*\right] = \frac{1}{2\eta}\bar{E}(r,\theta,\phi)^2 \qquad (2.52)$$

Where E represents the electric field intensity, H refers to the magnetic field intensity, and η is the intrinsic impedance of the transmission medium.

2.2.4 Radiation Intensity

Antenna radiation power per unit solid angle is defined as the radiation intensity, U (W/unit solid angle) [24], as expressed in the following equation:

$$U = r^2 \mathrm{P}_r \tag{2.53}$$

In the above equation, r is the distance to the antenna. The total power radiated by an antenna, P_{rad}, is obtained by integrating the radiation intensity over the entire solid angle of 4π, as given in the following equation:

$$\mathrm{P}_{rad} = \oiint_{\Omega} U d\Omega = \int_0^{2\pi} \int_0^{\pi} U \sin\theta d\theta d\phi \tag{2.54}$$

Where dΩ is the element of solid angle.

2.2.5 Directivity

The antenna directivity is the ratio of a radiation intensity towards a particular direction, to the average radiation intensity over all directions [26]. The average radiation intensity is estimated using the total power radiated divided by 4π. The directivity of a non-isotropic antenna is the ratio of its radiation intensity in a specified direction over that of an isotropic antenna, as expressed in the following equation:

$$D = \frac{U}{U_0} = \frac{4\pi U}{\mathrm{P}_{rad}} \tag{2.55}$$

In the previous equation, P_{rad} is the total radiated power. When the direction is not clarified, the antenna directivity means the direction of maximum radiation intensity [24].

$$D_{\max} = \frac{U_{\max}}{U_0} = \frac{4\pi U_{\max}}{P_{rad}} \tag{2.56}$$

2.2.6 Gain

The gain of an antenna is the ratio of radiation intensity in a specified direction, to the radiation intensity from an isotropic radiator with the same power fed to it. The isotropic radiation intensity equals the antenna input power divided by 4π [25]. Comparing to the antenna directivity, the antenna gain parameter also takes into account the antenna efficiency and directional capabilities. The following equation describes the gain calculation [24]:

$$Gain = 4\pi \frac{Radiation\ Intensity}{Total\ Input\ Power} = 4\pi \frac{U_{(\theta,\phi)}}{P_{in}} \tag{2.57}$$

The relationship between antenna radiation, gain and directivity are described in the following equation in which, e_{cd} stands for radiation efficiency:

$$G_{(\theta,\phi)} = e_{cd} D_{(\theta,\phi)} \tag{2.58}$$

2.2.7 Efficiency

The total antenna efficiency e_o is utilised to describe losses at the input terminals and within the antenna structure. The losses are generally caused by two mechanisms, which are reflections due to the mismatch between an antenna and its transmission line and conduction and dielectric losses (I^2R). Figure 2.17 [24] illustrates the antenna terminals and losses.

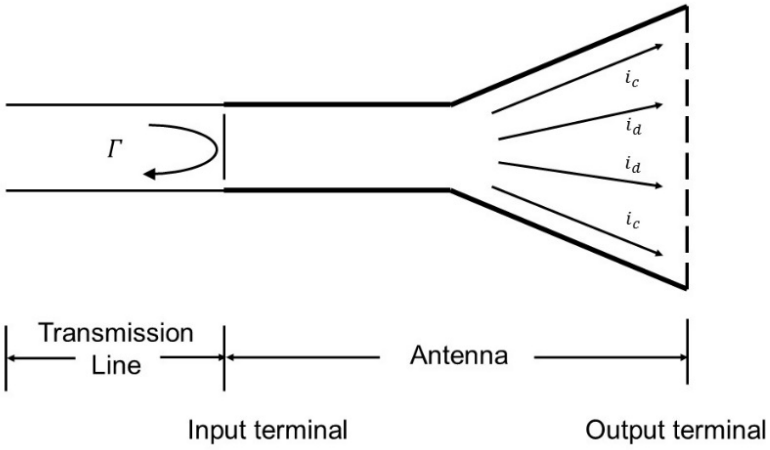


Figure 2.17. Antenna terminals and losses.

The total efficiency e_o is calculated by using the following equation:

$$e_0 = e_r e_c e_d \tag{2.59}$$

Where e_r is the reflection (mismatch) efficiency and $e_r = (1 - |\Gamma|^2)$, Γ stands for the voltage reflection coefficient at the antenna input terminals that can be calculated using the following equation:

$$\Gamma = (Z_A - Z_C) / (Z_A + Z_C) \tag{2.60}$$

Where Z_A is the antenna input impedance, and Z_C is the characteristic impedance of transmission line. In equation (2.59), e_c represents the conduction efficiency and e_d describes the dielectric efficiency.

The Voltage Standing Wave Ration is calculated by:

$$VSWR = \frac{1+|\Gamma|}{1-|\Gamma|} \tag{2.61}$$

Antenna radiation efficiency e_{cd} is calculated by using the following equation:

$$e_{cd} = e_c e_d = \frac{P_{rad}}{P_{in}} \tag{2.62}$$

Where P_{rad} is the total radiated power and P_{in} is the total input power to the antenna.

2.2.8 Polarization

Antenna polarisation describes the instantaneous electric field orientation of the propagated electromagnetic wave. It is a far-field characteristic of electromagnetic waves radiated by all practical antennas. In general, polarisations can be categorised into linear, circular, or elliptical. In the linear polarized mode, the electric field vector is always directed along a line. If the antenna radiates an electromagnetic wave in a corkscrew pattern and performs a complete revolution in each wavelength, this radiation is defined as circular polarisation. The figure of the electric field is traced either clockwise that known as RHCP, or counter-clockwise that known as LHCP. When the electric field traces is an ellipse, the radiation is classified as elliptical polarisation. Linearly and circularly polarised antenna patterns are special cases of elliptical polarisation, and they can be achieved when the ellipse becomes a straight line or a circle, respectively [24].

2.3 Antenna Array Fundamentals

The radiation pattern of the individual antenna element cannot be controlled easily. However, the possibility of significantly changing the pattern can be achieved by combining the outputs of multiple antenna elements. Such a group of multiple radiating elements, positioned in a way to a maximum radiation into a certain direction is known as an array antenna [24].

The radiation pattern of a single element antenna is usually wide and has a relatively low-directivity [27]. To meet the demands of long communication links, it is recommended to design an antenna with high directivity. This can be achieved by modifying the electrical size of the antenna that leads to enhancing the directivity. An alternative way to meet high directivity is to design an antenna array. The radiation pattern of the array is obtained by the vector addition of the radiation pattern of each individual element, taking into consideration the mutual coupling among the elements.

Array analysis begins using isotropic point sources. The isotropic receiving or transmitting element receives or transmits equally in the three dimensions. By using a simple multiplication process, the full pattern of the real antennas used as elements can then be included. Full array analysis involves summation of the phasors representing the amplitude and phase of each element. The pattern of an array of isotropic elements is called the array factor, which must be multiplied by element pattern to obtain the full pattern in real antenna array [24, 28, 29].

The first example for a simple antenna array configuration is an array consists of two isotropic sources with identical amplitude and phase signals in free space. These isotropic sources are placed horizontally along the z-axis and spaced apart by one-half wavelength. The radiation pattern for this array can be approximated by inspection as shown in Figure 2.18 [30].

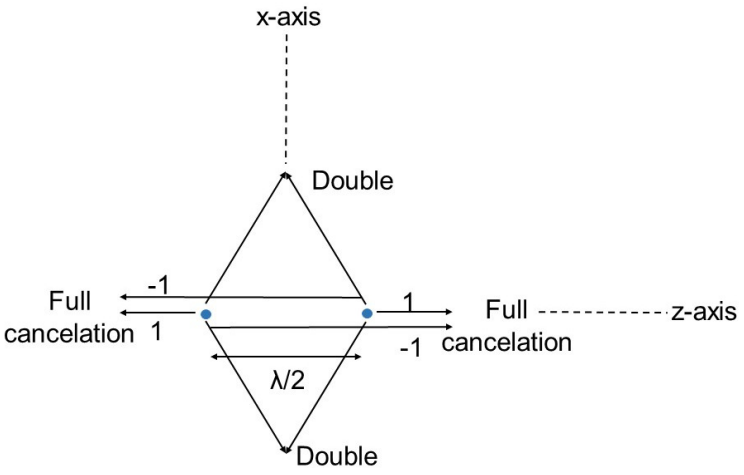


Figure 2.18. Pattern approximation of two isotropic sources separated by λ/2 with identical amplitude and phase using the inspection method.

The path length for each source is equal to each point on the x-axis in the far-field region. Since the amplitude and the phase are equal, the waves arrive equally in amplitude and phase so that the total field is doubled at each point. The situation is different along the z-axis, which is the axis of the array. The waves need to travel one-half wavelength coming from the left source before reaching the source on the right, which causes a 180° phase lag. The waves then continue travelling to the right along the positive z-axis with maintaining this out of phase relationship. Due to the sources having equal amplitude signals, then a perfect cancellation is archived along with the z-axis in both directions. Then the total

pattern has a relative value of two in the x-direction and zero in the z-direction with a smooth variation in between due to the smooth change in phase difference between waves between 0 and 180° as the observer moves from the broadside direction to the axial direction along a constant radius from the array centre. The two dimensional (2D) and the three dimensional (3D) polar patterns are shown in Figure 2.19 [30].

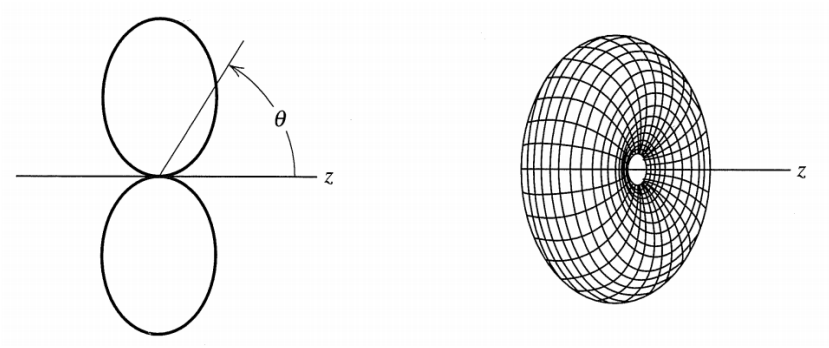


Figure 2.19. The 2D and 3D radiation pattern of two isotropic sources separated by $\lambda/2$.

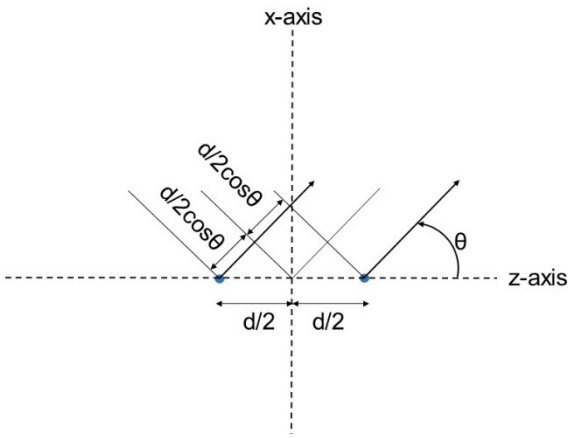


Figure 2.20. Geometry for pattern calculation using rays.

The array factor (AF) can be calculated exactly by using phases corresponding to the path length differences shown in Figure 2.20 [30]:

$$AF = 1e^{-j\beta(d/2)\cos\theta} + 1e^{j\beta(d/2)\cos\theta} = 2\cos(\beta\frac{d}{2}\cos\theta) \tag{2.63}$$

While the distance d between the elements is λ/2 and β is the propagation constant that is equal 2π/λ, then βd/2=π/2 and equation (2.63) becomes:

$$AF = 2\cos(\frac{\pi}{2}\cos\theta) \tag{2.64}$$

Normalizing the array factor for a maximum value of unity gives:

$$f(\theta) = \cos(\frac{\pi}{2}\cos\theta) \tag{2.65}$$

Equation (2.65) shows that the maximum can be achieved when θ=π/2 and the minimum (0) when θ equals zero that is shown in Figure 2.19.

The second example for a simple antenna array configuration is an array consists of two isotropic sources with identical amplitude and opposite phase signals in free space. The gross features of the pattern can be determined by using the previous inspection method as shown in Figure 2.21 [30]. The path length from each point source to a point in the x-axis is the same. However, one of the sources is out of phase by 180°, thus the waves arriving at all points in the x-axis

with a 180° out of phase and equal in amplitude. Along both directions of the z-axis, the 180° phase difference in the waves is compensated by the λ/2 path difference between the two sources. The entire pattern can be sketched in the 2D and 3D as shown in Figure 2.22 [30].

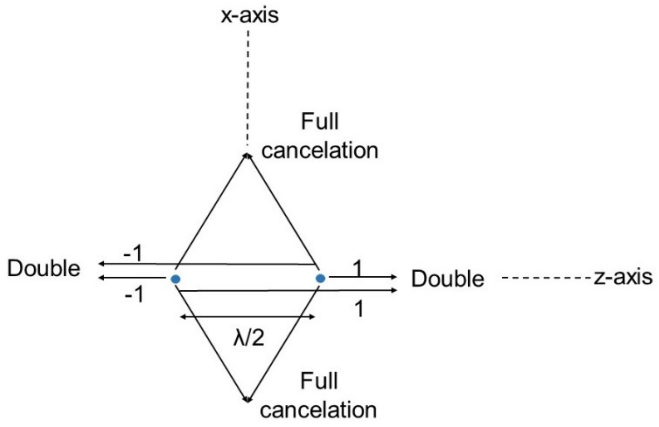


Figure 2.21. Pattern approximation of two isotropic sources separated by λ/2 with identical amplitude and opposite phase using the inspection method.

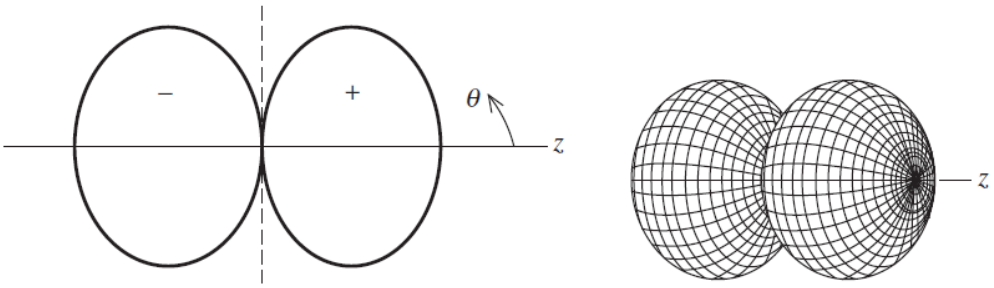


Figure 2.22. The 2D and 3D radiation pattern of two isotropic sources with identical amplitude and opposite phase separated by λ/2.

2.4 Full Duplex Communication Fundamentals

WLAN communication is usually using half-duplex mode on a single channel for communication applications [31-34]. In this mode, systems can send and receive at different times or frequencies to avoid the interference between the two signals. Frequency Division Duplex (FDD) and Time Division Duplex (TDD) are the two main techniques of half duplex mode, which are exploited in the current wireless systems [35]. Even though FDD and TDD improve communication systems, both techniques cannot be used to receive and transmit concurrently over an entire bandwidth that is assigned for a system [36]. Recently, the massive proliferation of wireless networks causes a spectrum shortage of the frequency band that has been assigned for wireless communication networks [37]. Therefore, there has been a considerable concern about a full duplex mode to be the future direction of wireless systems [37, 38]. The full duplex communication means the system can receive and transmit on the same frequency at the same time. Consequently, the spectral efficiency will be doubled theoretically. In addition, it can solve some problems, such as large end-to-end delays and eliminating the hidden terminal issue [39].

The associated problem that prevents the fulfilment of a practical full duplex mode is the self-interference signal. This signal is generated by the transmit antenna of the same node, and it is received by the receive antenna with the desired signal that comes from a different node [37]. Due of the space between the receiving and transmitting antennas are so small compared to the distance between the two nodes, the power of the self-interference signal is tens of decibels higher than the desired signal [40, 41]. The concern about cancelling the self-interference

signal has been rising recently. Many methods have been suggested in order to cancel or reduce the self-interference signal. These techniques are categorized into three main groups, which are an antenna, analogue and digital cancellation techniques [39, 42-44].

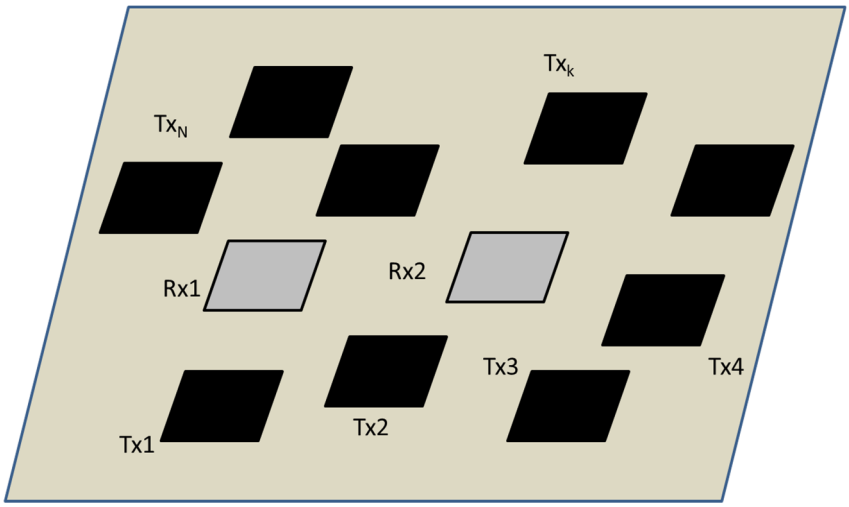


Figure 2.23. Antenna cancellation technique diagram.

Antenna cancellation technique is achieved by using more than one transmitting or receiving antenna. These antennas are structured in such a way to force the transmitted signals to cancel each other at the receiving antennas [42]. To demonstrate the cancellation technique, a simple structure of a full duplex system is shown in Figure 2.23, which shows many transmitting antennas and two receiving antennas. For this structure, the input received signal at Rx1 could be given by:

$$R_x = \sum_{i=1}^{n} h_i(t) * s_{ti}(t) \tag{2.66}$$

Where i is the index of the transmitter signal, n is the total number of transmitters, $h_i(t)$ is the i^{th} channel between the transmitter i and the receiving element and the $*$ is the convolution operator between two signals.

The transmitting signal could carry one or multiple signals. This could be expressed for both assumptions in which the signals arrive at the receiver with different time delay and phase shift corresponding to the distance between the transmitter and the receiver antennas. Controlling the phase shift could also be embedded into the transmitter signal to force the cancellation at the receiver. From that concept, signals from two transmitters could be cancelled if they are arranged out of phase with an acceptable equal amplitude at the receiving antenna. It is important to know that this depends on the distance between the transmitting antennas besides the attenuation caused by the channel between the transmitting and the receiving antennas. The lines joining the transmitting elements could be arranged in a way to be cancelled with a better attention of the channel attenuation that will be performed by the proper design of the feeding network.

In general, these arrangements have been used to simplify the cancellation of multiple transmitted signals and especially into the new full duplex of MIMO system; in which, antenna cancellation with asymmetrical antenna placement has been presented. The design consists of three antennas, two as transmitters, while the other one as a receiver, which is placed between the two transmitters. The distance between the first transmitter and the receiver is d, whereas the second transmitter is placed at distance of $d+\lambda/2$ away from the receiver. The aim of

adding an extra distance of λ/2 for the second transmitter antenna is to make the second transmitted signal cross an extra distance to reach the receiver. As a result, there will be a 180˚ phase difference between them, and will eventually cancel each other at the receive antenna. This method can reduce the self-interference signal by up to 30 dB. The method in [39] has a limitation in terms of bandwidth and size. Firstly, the suggested idea relies on placing one transmitter by an extra distance of λ/2 to destruct the two transmitted signals at the receiver. The wavelength is calculated using a single frequency. Consequently, the design worked perfectly at that frequency, which has been used to find λ, and the performance degraded when moving away from that frequency. Thus, the system cannot provide high and stable cancellation over a wide frequency band. Additionally, adding extra λ/2 distance produces a larger antenna structure that possibly could not be fixed into some wireless devices.

Antenna cancellation with symmetric antenna placement has been proposed in [43], in which two transmitters with one receiver are utilized. The distances between the transmitting and the receiving antennas are equal. The original signal was divided into two symmetric signals in amplitude and phase. One of these two signals was connected directly to one of the transmitters, while the other signal passed through a 180˚ phase shifter. Therefore, the two signals arrived at the receiver with a 180˚ phase difference and added destructively.

This design has many benefits comparing it with the method in [39], Firstly, the idea of using a phase shifter to create the phase difference instead of adding extra distance to one of the transmitting antennas leads to providing higher

cancellation on a wider frequency band. Secondly, due to the two transmitting antennas are separated by an equal distance from the receiving antenna, studying channel behaviour and its effect on the transmitted signals is not required, because the impact will be the same on the two signals. Nevertheless, the insertion loss of the phase shifter that should be compensated in the other signal path, and the frequency response of the phase shifter is not flat over a wide bandwidth.

The second cancellation technique is known as the analogue cancellation, which is based on using the transmitted signal at the receive chain because the transmit chain is close to the receive chain. Therefore, a copy of the sent signal can be taken and subtracted from or added to the received signal. This process is achieved before the Low Noise Amplifier (LNA) in the RF domain [42].

Balanced / unbalanced (Balun) transformer with two antennas is utilized in [39]. The transmitted signal is divided into two signals that are similar in amplitude but have 180˚ phase difference between them. The transmitter is fed by one of these two signals for sending, whereas the second inverted signal is connected to the input of the tuning circuit. The goal of implementing the tuning circuit is to adapt and modify the phase and the amplitude of the inverted signal quickly, automatically and accurately, according to the second input of the tuning circuit, which is the received signal. After that, the inverted signal was added to the received signal to reduce the effect of the self-interference signal. The measurement showed that this technique provides a 45 dB cancellation over a 40 MHz bandwidth. However, it had some limitations such as suffering from

leakage or non-flat frequency response issue due to the inaccuracy of manufacturing of the Balun transformer. Additionally, the effects of the channel on the sending signal are ambiguous and not easy to compensate.

In [44], a single antenna with a circulator is suggested to cancel or reduce the self-interference signal. The antenna was used for sending and receiving, and the circulator to isolate these two signals. Therefore, there was no self-interference signal composited with the received signal. However, the circulator had a leaking problem between its ports. Hence, the port of the sending signal passed part of the signal to the port of the received signal. Results indicate that this design can provide around 75 dB cancellation on 10MHz bandwidth. Using noise canceler chip for cancelling the self-interference signal [45]. This chip can supply an extra 20 dB cancellation when adding it with other cancellation methods.

The third method for cancellation is known as the digital cancellation in which the generated baseband signal at the transmitter is subtracted or added to the output of the Analogue-to-Digital Converter (ADC) at the receive chain. Memory is utilized to store transmitted digital samples. After that, the amplitude and phase of these samples are modified to be similar or opposite to the sending samples, which exist at the received signal. Then, the subtraction will be applied between the adjusted samples and the received samples to remove the residual self-interference signal [42].

Chapter 3

Practical Power Divider Designs

Various Wilkinson power divider structures are investigated and characterised in this section. They differed in dimensions, fabrication materials, and integration methods. A miniature equal split structure is presented, in order to construct a suitable feeding network for antenna array systems. In addition, a general example for planar multi-output ports power divider is presented in this chapter as well. As mentioned earlier, Wilkinson power divider can be designed to provide arbitrary power division. Therefore, a reconfigurable output power Wilkinson power divider is also presented that can be tuned from equal to unequal output power operations.

3.1 Ultra-Wideband Power Dividers

This section presents the design of a 1 to 2 equal power and phase wideband Wilkinson power divider. Different structures are studied, designed and optimised and their performance compared to select the smallest structure.

The design parameters for the quarter wave transformers and isolation resistors can be obtained with reference to look-up tables and charts [23, 46, 47]. The initial design data for the ports and quarter wave transformer impedances and resistor values used in the three following designs are listed in Table 3.1 considering 3.5 GHz as a central frequency. The following power dividers are fabricated on a 0.8 mm thick FR-4 substrate with a dielectric constant of 4.3. The

line width and length structure parameters are calculated using equations (3.2) to equation (3.5) subject to $W/h \geq 1$ [48]. In which W represents the microstrip line width and h is the substrate thickness:

$$Z = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.97h}{0.8W + t}\right) \tag{3.1}$$

$$W = \frac{7.48h}{e^{\frac{Z\sqrt{\varepsilon_r + 1.41}}{87}}} - 1.25t \tag{3.2}$$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + \frac{12 \times t}{W}}} \tag{3.3}$$

$$\lambda_e = \frac{3 \times 10^8}{f_0 \sqrt{\varepsilon_e}} \tag{3.4}$$

$$L = \lambda_e / 4 \tag{3.5}$$

In these equations, Z is the characteristic impedance of the microstrip transmission lines, ε_e is the effective relative permittivity of the substrate, λ_e is the effective wavelength and f_0 is the centre frequency, which is 3.5 GHz for this design. The bisection line of all ports and quarter wave sections is considered to be the equivalent microstrip line length to simplify the design. The gap between branches of the power dividers fixed to be 1.4 mm to use a 0805 size SMD thin film resistor.

Table 3.1. The initial dimensions for the three-sections UWB power divider.

	Z (Ω)	R (Ω)	W (mm)	L (mm)
Input (port 1)	50	-	1.52	11.86
Section 1	90.52	96.1	0.43	12.49
Section 2	70.71	94.3	0.79	12.22
Section 3	55.24	527	1.28	11.96
Output (ports 2 &3)	50	-	1.52	11.86

Three different geometries are illustrated to find the smallest structure with acceptable performance. The initial S-parameters before and after optimisation are presented. The optimised values that used in fabricating the power dividers are given. The fabricated prototypes are shown with overall power divider dimensions. The measured S-parameters are compared with simulation results to validate the designs.

3.1.1 Straight Three Sections UWB Power Divider

The first studied geometry is designed by using three sections of straight quarter wave transformer to create a 1 to 2 UWB power divider with an equal split, which is shown in Figure 3.1. The initial design parameters are listed in Table 3.1. The FR-4 substrate used for this design, which has a copper thickness of 35 µm. This particular substrate is selected due to its cheap price and the ease of the fabrication process.

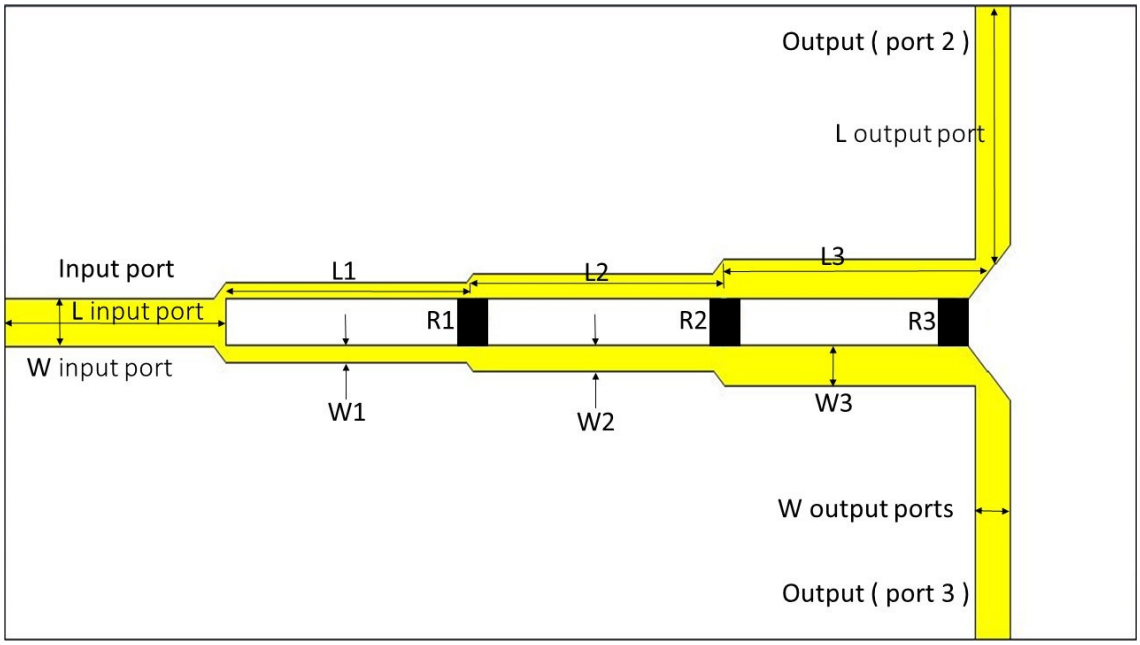


Figure 3.1. The schematic of the straight three sections equal split UWB power divider.

Figure 3.2 shows the initial simulated S-parameters for the power divider. Desired results are achieved for input port return loss that is better than 10 dB from 88 MHz to 7.72 GHz and an insertion loss of 3.6 dB at 3.5 GHz but it is below 5 dB at higher frequency band for the operational bandwidth. Due to the structure symmetry and to simplify the figures, only the return loss of the input port and one of the output ports are shown with the isolation between output ports. The initial output port return loss is better than 10 dB from 63 MHz to 7.42 GHz. While output ports isolation is better than 10 dB from 90 MHz to 8.15 GHz. The operational bandwidth of this power divider is 6.86 GHz.

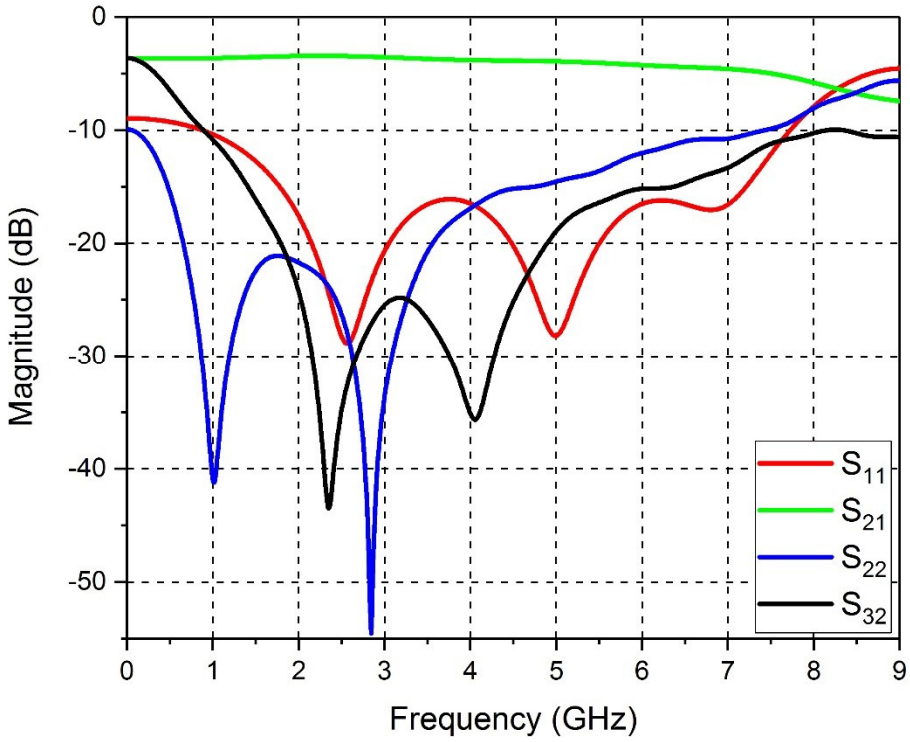


Figure 3.2. Initial simulated S-parameters for the straight three sections UWB power divider.

To enhance power divider performance and reduce the size, the Particle Swarm Optimisation algorithm (PSO) is used. This algorithm has been reported that it is suitable for models with many optimized parameters and it can give better and faster optimum results [49]. The power divider input and output ports length and width and, quarter-wave transformer sections lengths and widths are optimised with a goal to achieve a return loss better than 25 dB. The optimised design parameter values are shown in Table 3.2.

Table 3.2. The optimised design parameters for the straight three sections UWB power divider.

	R (Ω)	W(mm)	L(mm)
Input (port 1)	-	1.42	8.78
Section 1	60	0.48	9.83
Section 2	126	0.75	9.99
Section 3	282	1.18	9.98
Output (ports 2 &3)	-	1.42	8.78

The optimised structure S-parameters are shown in Figure 3.3. It is clear that the enhancement in both bandwidth and input port return loss are achieved. The input port return loss becomes better than 10 dB from 0.5 to 7.6 GHz. No change was observed for the insertion loss as it is related to the substrate properties [50], which has not been changed. Output port return loss is also enhanced and become better than 10 dB from 98 MHz to 8.38 GHz. A slight improvement was achieved in terms of output ports isolation that become better than 10 dB from 1.07 to 8.68 GHz. The operational bandwidth of the optimised power divider is 7.1 GHz compared to 6.8 GHz before optimization.

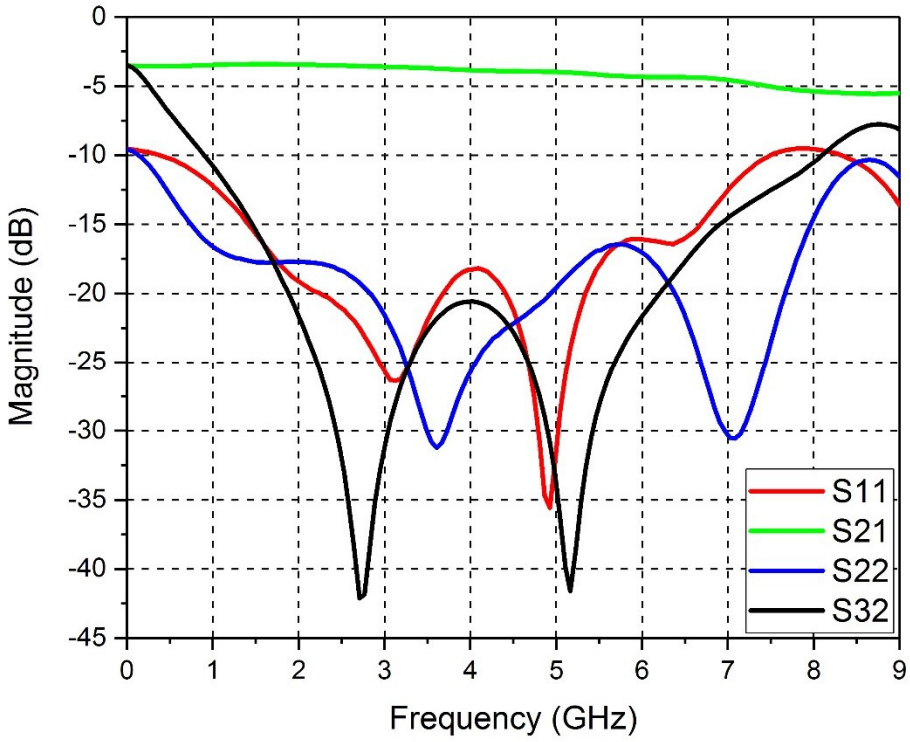


Figure 3.3. The optimised S-parameters for the straight three sections UWB power divider.

A size reduction is also achieved after optimisation as the optimised power divider size is 19 mm $\times$ 45 mm compared to 25.1 mm $\times$ 40 mm before optimisation, which means a 14.8 % reduction in size. Figure 3.4 shows the fabricated prototype. The bottom layer of the power divider is a full ground. For practical reasons, R1, R2 and R3 are selected to be 35.7, 127 and 280 Ω respectively, and a '0805' package size is selected.

Figure 3.5 shows the measured S-parameters for the power divider. There is a difference between measurements and simulation results in the magnitude but the overall response are both agreed.

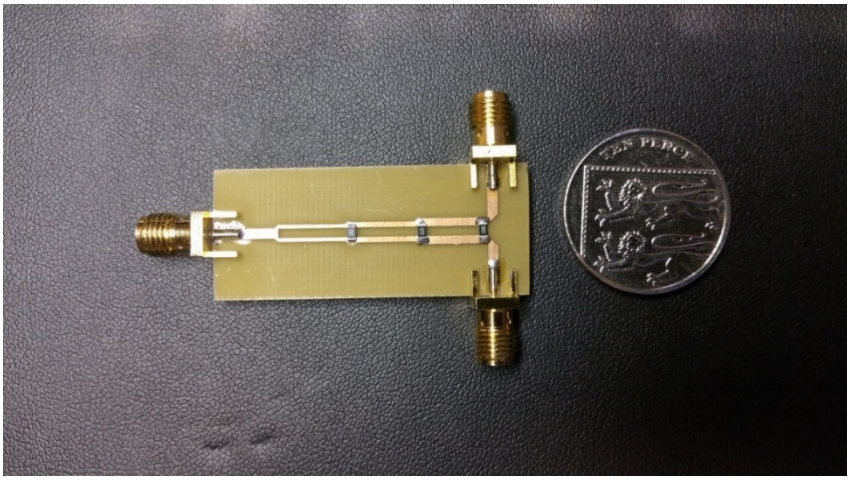


Figure 3.4. The fabricated board of the straight three sections UWB power divider.

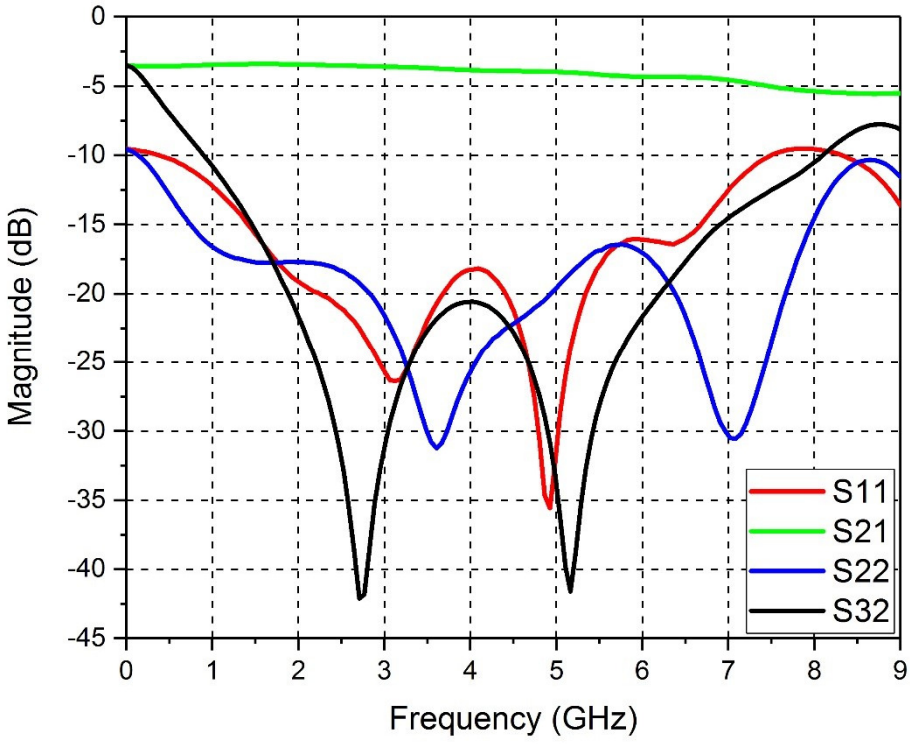


Figure 3.5. The measured S-parameters for the straight three sections UWB power divider.

3.1.2 Mitred Microstrip Line Three Sections UWB Power Divide

The second geometry is a mitred microstrip line 1 to 2 UWB power divider structure that shown in Figure 3.6. The aim is to design a smaller size power divider by bending the quarter wave transformers. In general, microstrip circuits are easy to fabricate and allow the convenient integration of passive components [51]. Almost any types of microwave circuits and subsystems can be made in microstrip form. However, microstrip lines are associated with discontinuities problem that causes circuit performance degradation, due to junctions, step changes in line width and line bends [52]. This is because such discontinuities change the line characteristic impedance by introducing shunt capacitance, which can lead to phase and amplitude changes and input and output mismatch by increasing reflection level from those discontinuities [53, 54].

Bends are the most frequently used discontinuity. However, due to the excess capacitance at a square corner of the bend, the characteristic impedance value will be lower than that of the uniformly connected lines. In addition, the effective length of the bent microstrip line becomes shorter than the designed length [55]. The bend discontinuity effect will increase with frequency, with the number of bends used in cascade, and with the line width [56].

One of the approaches to minimize the effect of bends is by compensating the discontinuity directly often by chamfering or mitring the conductor at the corner. Several equations are reported for mitring, such as the perfect mitring [55], the 1.6 ratio mitring [23] and the 1.8 ratio mitring [2]. The length of the mitre in the perfect mitring method is equal to the width of the microstrip line; while in the 1.6

and 1.8 mitring ratio methods are equal to 1.6 and 1.8 times the microstrip line width respectively. The increased conductor area at the corner of the bend cause a parasitic discontinuity capacitance, which can be reduced by mitring the corners [57].

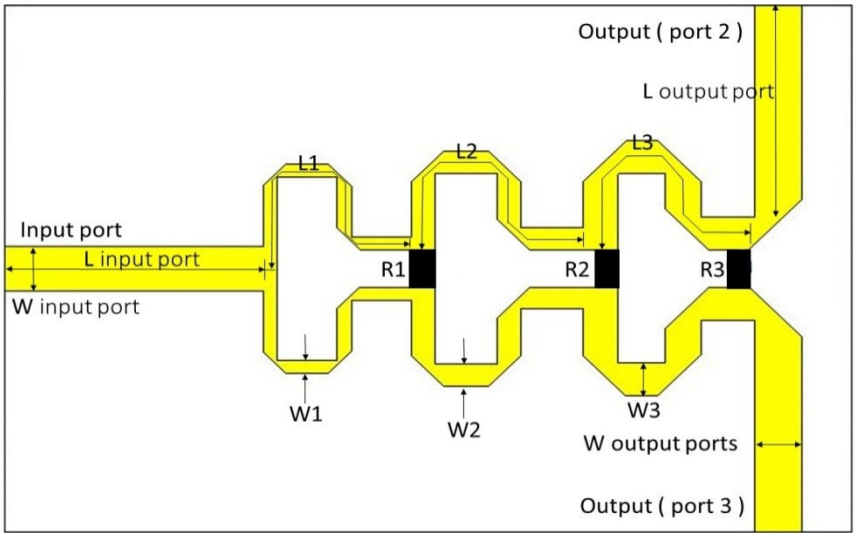


Figure 3.6. The schematic of the mitred three sections equal split UWB power divider.

The same initial design parameters that used in the first structure were used with this power divider, which are shown in Table 3.1. Figure 3.7 shows the initial simulation results of the S-parameters. The return loss of the input port is better than 10 dB for a bandwidth of 5.4 GHz from 0.6 to 6 GHz and the insertion loss is between 3.6 and 6 dB for the same bandwidth. The output ports return loss is better than 10 dB from 90 MHz to 7.3 GHz while the output ports isolation is better than 10 dB from 74 MHz to 6.4 GHz.

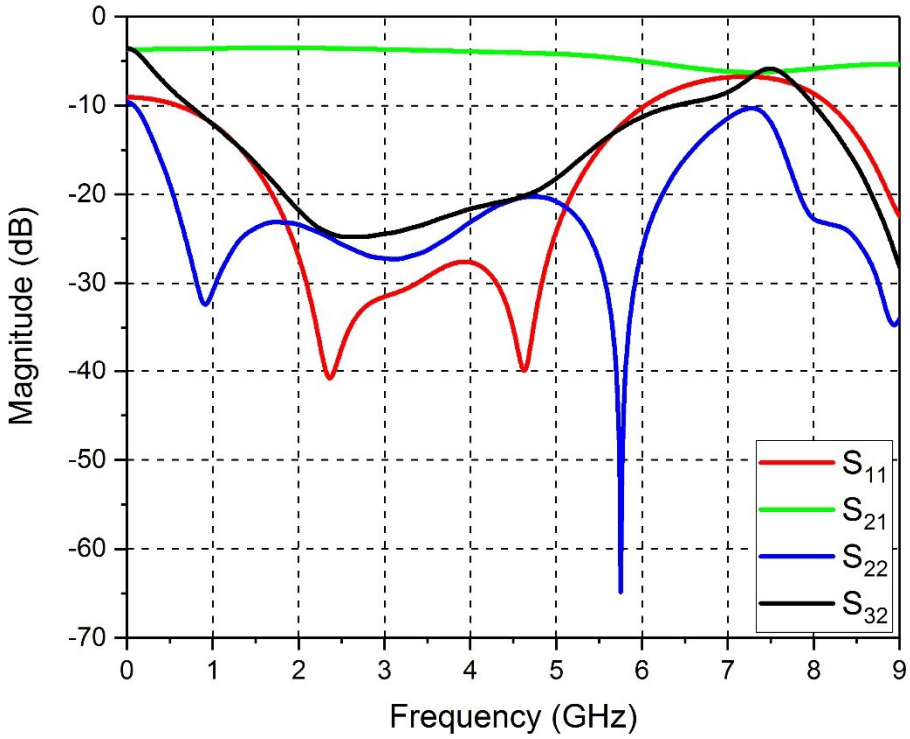


Figure 3.7. The initial simulation S-parameters of the mitred UWB power divider.

The same optimisation algorithm that has been used in the previous design was used to enhance power divider performance and reduce the size. The power divider input and output ports width and length, quarter-wave transformer sections widths and length are optimised to achieve that goal. The optimised design parameters are listed in Table 3.3.

The optimised S-parameters values are shown in Figure 3.8, which shows a good enhancement in both bandwidths and return loss values. The input port return loss bandwidth becomes wider. A 6.97 GHz bandwidth is achieved from 77 MHz to 7.3 GHz and the output ports return loss is from 81 MHz to 8.85 GHz. Adding to that, the output ports isolation is also enhanced and become better than 16 dB for the operational band. The insertion loss is not changed as it is related to the conductor and dielectric losses of the substrate [50].

Table 3.3. The optimised dimensions for the mitred three sections UWB power divider.

	R (Ω)	W (mm)	L (mm)
Input (port 1)	-	1.66	9.16
Section 1	36	0.49	10.42
Section 2	128	0.83	10.17
Section 3	280	1.25	9.03
Output (ports 2 &3)	-	1.66	9.16

The new dimension of the optimised power divider is 20 mm $\times$ 31 mm, which is 26% smaller compared to the power divider before optimisation that has a 25.1 mm $\times$ 33.4 mm dimensions. Figure 3.9 shows the top layer of the fabricated prototype. The power divider has a full ground that is not showing in Figure 3.9. The same SMD resistor values and the package size of the previous geometry were used.

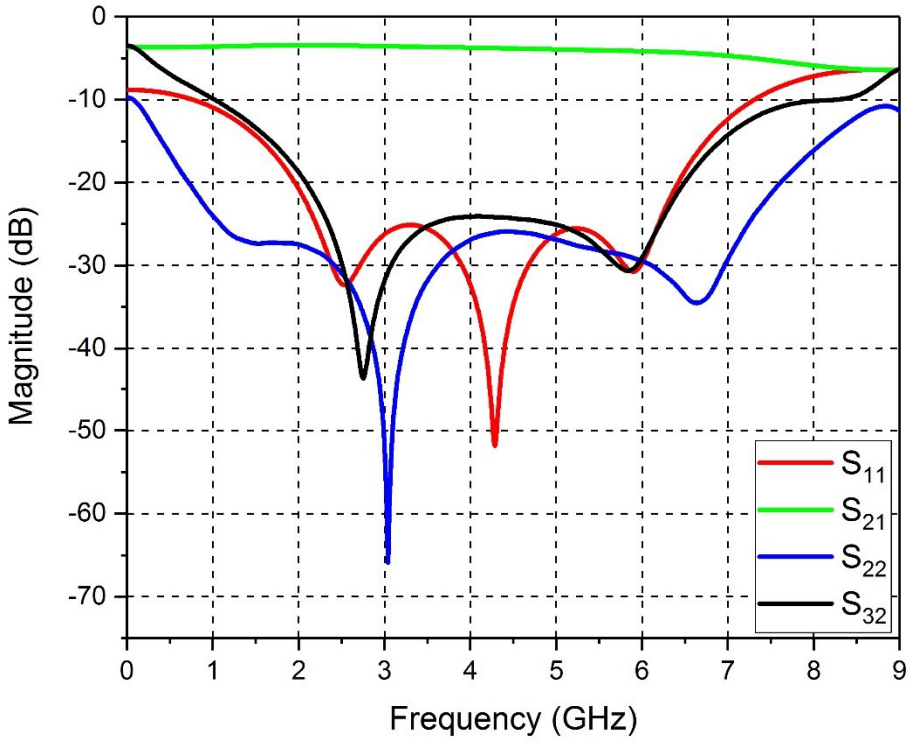


Figure 3.8. The optimised S-parameters of the UWB mitred power divider.

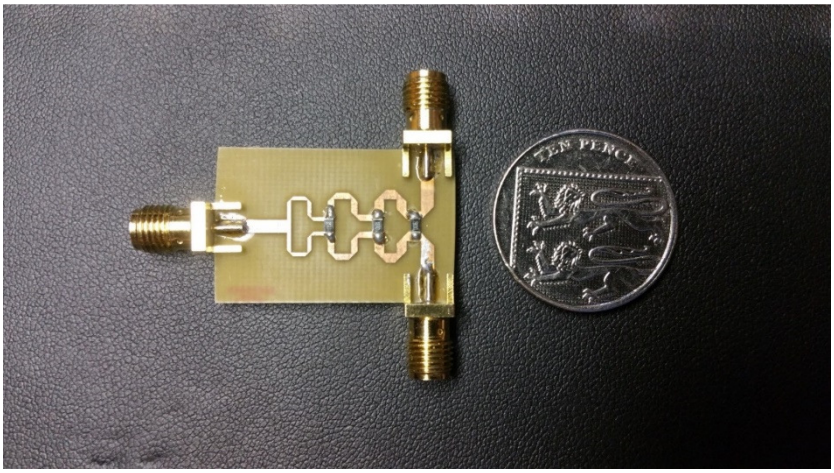


Figure 3.9. The fabricated board of the mitred three sections equal split UWB power divider.

Figure 3.10 shows the measured S-parameters. Comparing Figure 3.10 with Figure 3.8, a good agreement can be absorbed. The input port return loss is better than 10 for almost the same bandwidth from 60 MHz to 7 GHz. The

difference between the measured and simulated results could be due to not simulating the SMA connectors and could be due to the inconsistent amount of soldering that has been used for the SMA connectors and SMD resistors.

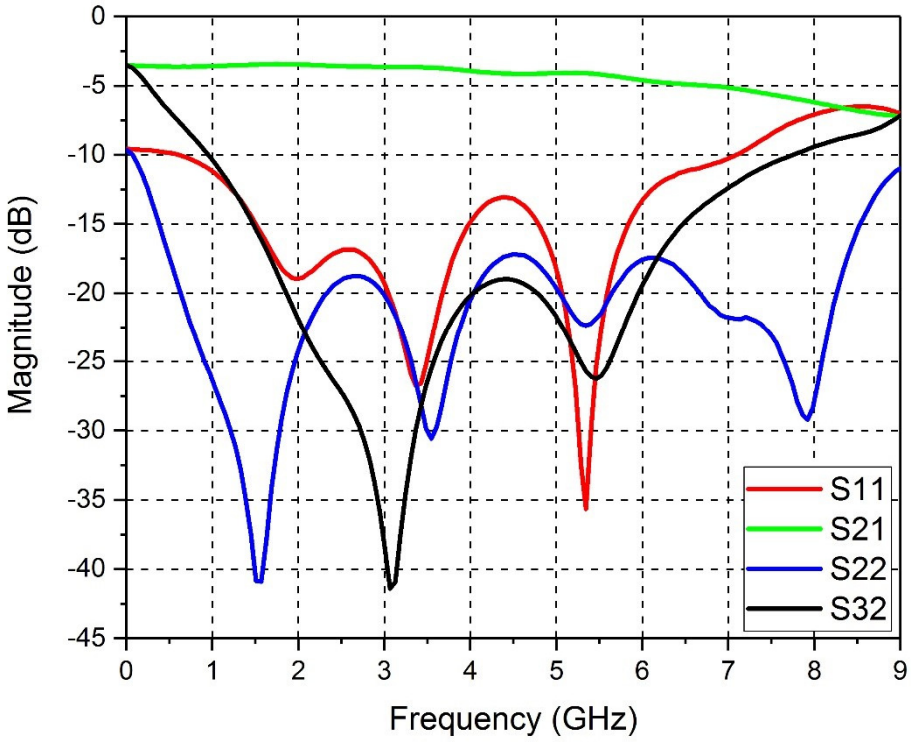


Figure 3.10. The measured S-parameters for the mitred three sections UWB power divider.

3.1.3 Circular Three Sections UWB Power Divider

Another approach for eliminating the effect of a discontinuity is by bending the microstrip line with a smooth curved line that has a radius equal or greater than three times of the microstrip line width, but this takes up more space [2, 23]. The third studied geometry is a three sectioned 1 to 2 UWB power divider with circularly shaped quarter wave transforms. The schematic diagram of this power divider is shown in Figure 3.11. The same initial design values are used that have

been used with the previous designs, which are listed in Table 3.1. To construct circular sections, the radius of circles are calculated by considering the section length to be the bisection line of the circular section. Taking into consideration the SMD resistor gap in the first section radius calculation as the gap should be reduced from the circle radius. The following equations are used to calculate the three section radii:

$$First\ section\ redius = \frac{2 \times first\ section\ length - gap}{2\pi} \tag{3.6}$$

$$Other\ section\ redii = \frac{other\ section\ length}{\pi} \tag{3.7}$$

The values of section radii are 2.9, 3.18 and 3.18 mm for sections one to three respectively.

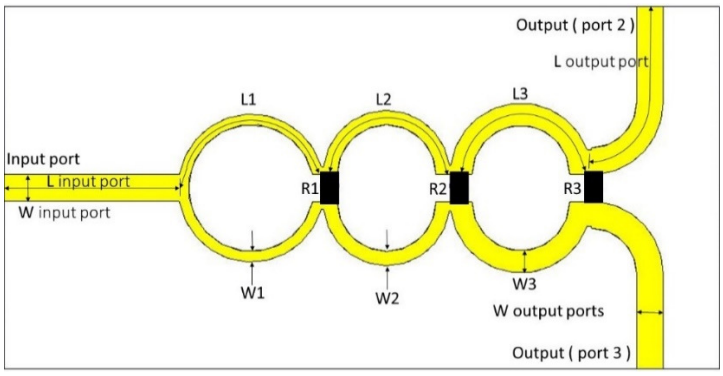


Figure 3.11. The schematic of the circular three sections equal split UWB power divider.

The initial simulated S-parameter results are shown in Figure 3.12, which shows that the return loss of the input port is better than 10 dB between 0.9 to 9.9 GHz

that means an operational bandwidth of 9 GHz. The insertion loss is between 3.6 dB and 5.4 dB for the same band. In addition, the plot shows that the output ports insertion loss is better than 10 dB between 125 MHz to 10.2 GHz while the isolation between output ports is 16.5 dB as a minimum for the same operational band.

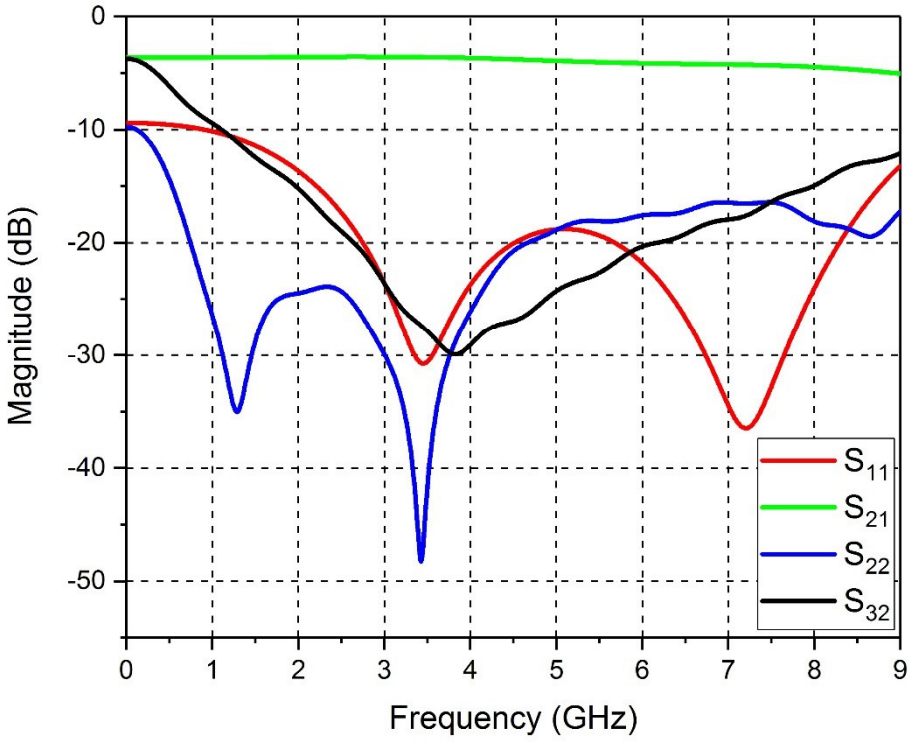


Figure 3.12. The simulated S-parameters for the circular three sections UWB power divider.

Same as with the previous power divider geometries, the PSO algorithm is used to obtain better performance and reduce power divider size. The power divider input and output ports width and length, quarter-wave transformer section radii and widths are optimised with a goal to achieve input port return loss better than 25 dB. The new optimised design values are listed in Table 3.4.

Table 3.4. The optimised dimension values for the circular three sections UWB power divider.

	R (Ω)	W(mm)	L (mm)	Radios
Input (port 1)	-	1.4	9.24	-
Section 1	104	0.55	9.66	3.88
Section 2	118	0.75	9.49	3.37
Section 3	318	1.13	9.33	3.75
Output (ports 2 &3)	-	1.4	9.24	-

The optimised power divider S-parameters are shown in Figure 3.13. Although the operational bandwidth is reduced and become 7.4 GHz from 600 MHz to 8 GHz, a return loss better than 25 dB is achieved for a bandwidth of 4 GHz from 2 to 6.5 GHz. An improvement is observed for the output ports return loss that becomes better than 10 dB from 90 MHz to 8 GHz and the isolation between output ports become better than 10 dB from 750 MHz to 8.2 GHz. The insertion loss did not change as it is related to the substrate properties, which are not changed similar to the previous geometries.

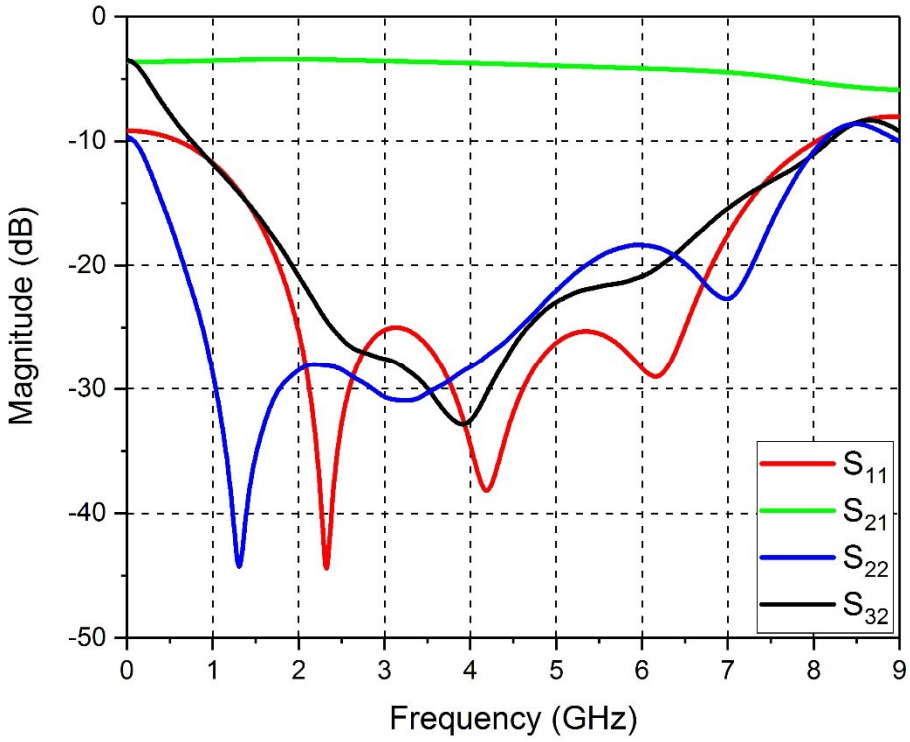


Figure 3.13. The S-parameters for the optimised circular three sections UWB power divider.

The optimised power divider structure is smaller in size. A 6.6 % size reduction is achieved by optimisation with an overall board size of 19 mm × 38 mm compared to 19.05 mm × 40.59 mm before optimisation. Figure 3.14 shows the upper layer of the fabricated prototype. The bottom layer of the power divider is also a full ground similar to the previous structures. For practical reasons, off-shelf resistors values for R_1, R_2 and R_3 are selected to be 105 Ω, 118 Ω and 360 Ω respectively and '0805' package size is used.

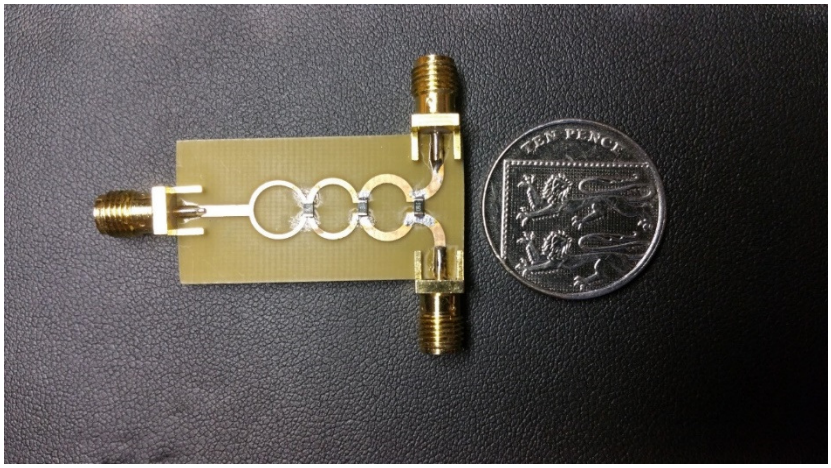


Figure 3.14. The fabricated board of the circular three sections equal split 1 to 2 UWB power divider.

Figure 3.15 shows the measured S-parameters in which a good agreement with simulation is observed. The slight difference in magnitude could be a reason to not considering the SMA connectors in simulation and the inconsistency in soldering the SMA connectors and the SMD resistors.

Comparing the performance and the size of the three designed power dividers, knowing that all of them achieved the desired UWB frequency band in terms of input and output ports return loss, insertion loss and isolation, the mitred geometry is more preferable to construct a small size and high-performance power divider. As the mitred structure is 29.8 % smaller than the linear structure and it is 16.8 % smaller than the circularly shaped quarter wave transformer structure. The operational bandwidth of the mitred power divider needs an extra optimisation to increase it, which will be achieved in the next section.

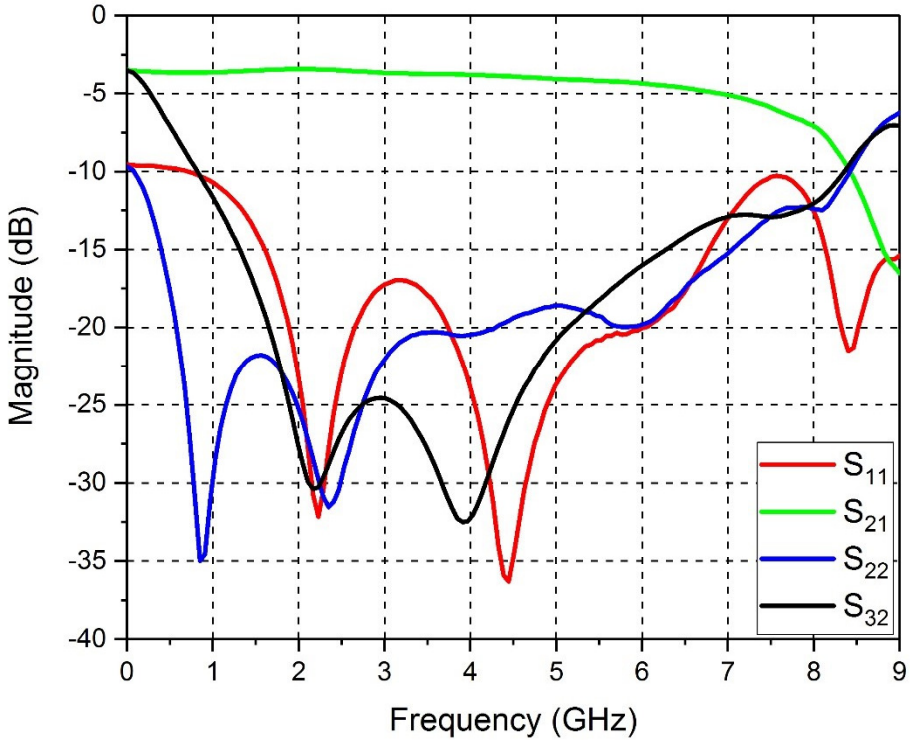


Figure 3.15. The measured S-parameters for the circular three sections UWB power divider.

3.1.4 Miniature UWB Power Divider

This section is based on a published paper [58]. The aim of this section is to design a miniature UWB power divider for antenna array feeding networks.

A miniature, lightweight, equal power and phase, four ports UWB Wilkinson power divider design is presented. A two ports UWB power divider simulated using CST microwave studio and optimised using PSO algorithm. The proposed power divider has promising S-parameters that covering the UWB from 3.1 to 10.6 GHz and it is physically small. The four ports power divider is constructed by using three of two ports power dividers by cascading two of them. All designs are fabricated on a Roger RO3035 substrate and are validated experimentally.

Generally, Wilkinson power dividers with single section structure are constructed from two quarter-wavelength transformers with 70.71 Ω impedance, which are terminated by a 100 Ω isolation resistor [10]. One method is widely used to expand the operational bandwidth of a narrow band power divider by adding additional quarter wave transformers. In this case, two additional quarter wave transforms have been added. These quarter wave transformers are terminated by isolation resistors with particular values [46]. The impedance of the quarter wave transformers and isolation resistors values can be found from charts and look-up tables [23, 46, 47].

Several numerical formulas can be used to find the microstrip characteristic impedance. Figure 3.16 shows a plot of the characteristic impedances with respect to microstrip line width using two methods. Equations (2.1) and (2.2) are given by IPC-2141 standard, which gives a good approximation for microstrip line width. While Sobol formula, equations (3.8) and (3.9), gave a better approximation for microstrip line width. The following equations are subject to W/h ≥ 1 [48].

$$Z_0 = \frac{377h}{W_{eff}\sqrt{\varepsilon_r}\left[1+1.735\left(\varepsilon_r\right)-0.0724\left(\frac{W_{eff}}{h}\right)^{-0.836}\right]} \tag{3.8}$$

$$W_{eff} = W + \frac{t}{\pi}\left[\ln\left(\frac{2h}{t}+1\right)\right] \tag{3.9}$$

The design parameters for the two ports power divider are listed in Table 3.5 for a centre frequency of 6.85 GHz. A 0.76 mm thick RO3035 substrate is used, which has a processed dielectric constant of 3.5 and a design dielectric constant of 3.6 and a copper thickness of 35 µm.

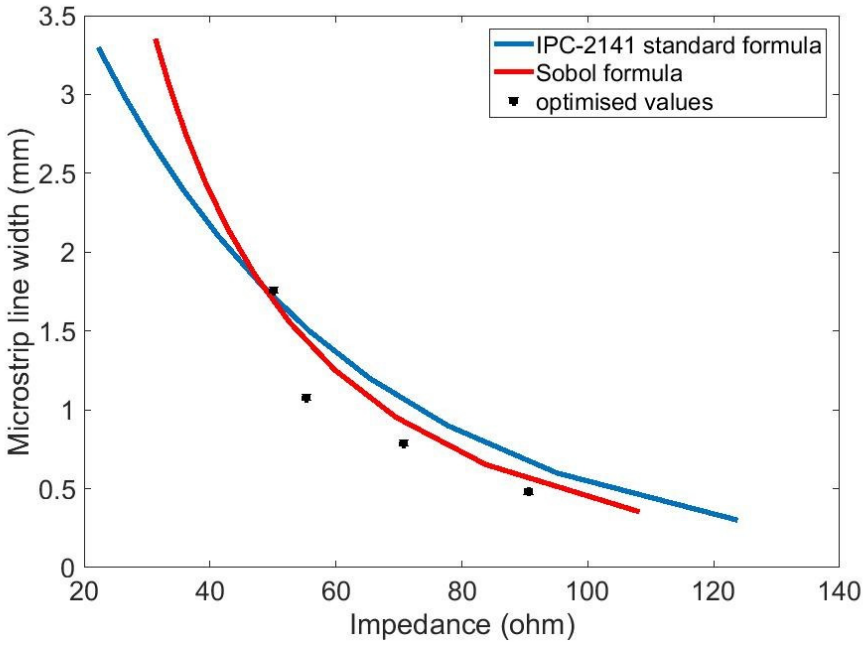


Figure 3.16. The characteristic impedance of quarter-wave sections with respect to microstrip line width calculated using two different methods.

Table 3.5 The initial design parameters for the 1-2 ports UWB power divider.

	Z (Ω)	R (Ω)	W (mm)	L (mm)
Input/output ports	50	-	1.69	6.656
First section	90.52	96.1	0.57	6.768
Second section	70.71	94.3	0.91	6.714
Third section	55.24	527	1.45	6.671

The bisection line of all microstrip lines considered the calculated length to simplify the design. A perfect mitring is used to reduce the high VSWR at the square corners caused by the excess capacitance [55].

The increment in the dielectric constant value reduces the wave propagation speed, that means the microstrip line length will be shorter compared to the same suspended microstrip line. This helps to reduce the structure size according to equation (3.5). However, it has a drawback of increasing conductor losses due to decreasing microstrip lines width as shown in equation (3.2). Besides that, a substrate with a high dielectric constant has a higher coupling and a lower radiation loss [59]. So that, the selected substrate based on considering all mentioned factors to have lower losses and smaller size.

Generally, there are two types of material used in substrates fabrication, Poly Tetra Fluoro Ethylene (PTFE) and thermoset materials. PTFE materials are less affected by humidity while thermoset materials are more stable thermally but more affected by ageing [60].

Electrode deposit and rolled copper production methods are the most common methods used to produce the copper sheet of the substrate. Generally, electrode deposited copper has a rougher surface, which means a better boundary connection between the copper sheet and the dielectric but increases conductor loss due to increasing surface roughness. On the other hand, rolled copper has a smoother surface, reducing conductor loss but weakening boundary connection with the substrate [59].

The selected substrate should offer good electrical, mechanical, thermal stability with small size and high performance. The substrate should be selected based on equations (3.2) and (3.9) in which the microstrip width is directly related to the thickness of the substrate and inversely related to the dielectric constant of the substrate. Taking all of that into consideration helps to fabricate a sufficient microstrip line width, which should be wide enough to reduce the effect of minor imperfections in fabrication [61].

CST Microwave studio is used with its optimisation toolbox to carry out a full wave analysis for the power dividers. Figure 3.17 shows the initial simulated S-parameters for the two ports power divider. The return loss is better than 10 dB over the operational band and the isolation is better than 14 dB. The insertion loss is between 3.2 and 3.8 dB across the desired band while the output ports return loss is not satisfying the requirements. To enhance the performance, PSO algorithm is applied with a goal of achieving a return loss better or equal to 20 dB over the operational bandwidth by optimising sections, ports length and width.

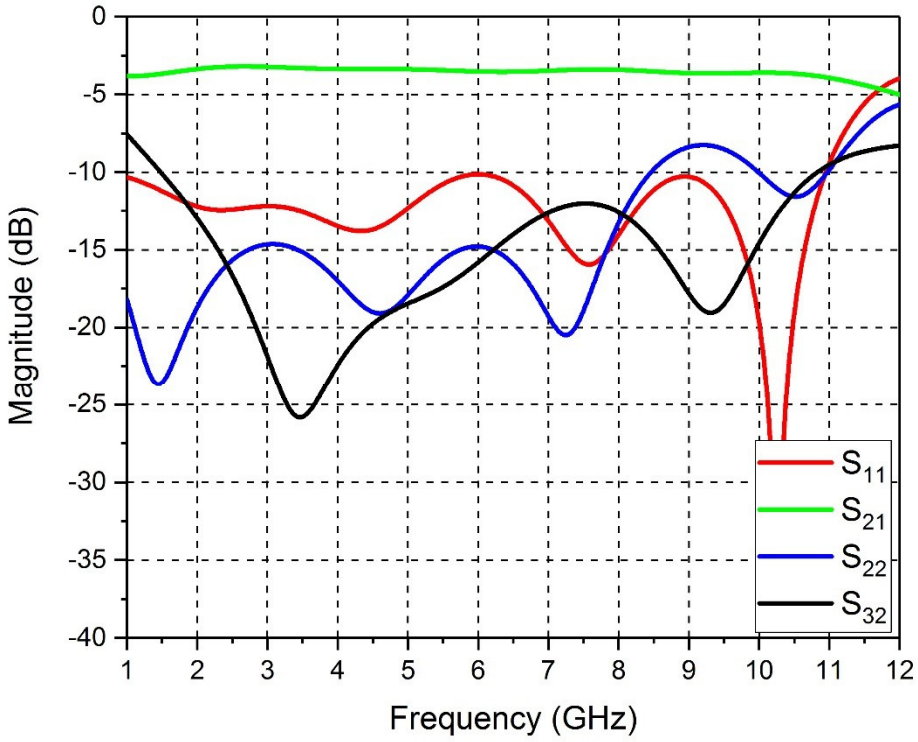


Figure 3.17. Initial simulated S-parameters for the miniature two ports UWB power divider.

The S-parameters for the optimised two ports UWB power divider are shown in Figure 3.18, which shows a significant improvement in return loss performance by a 7.5 dB and more than 2 dB in isolation. The insertion loss remains unchanged since it is a function of the copper surface roughness and the tangent loss of the substrate [26], both unaltered in this optimisation. Figure 3.19 shows the layout for the power divider with an overall size of 13 mm × 19.5 mm.

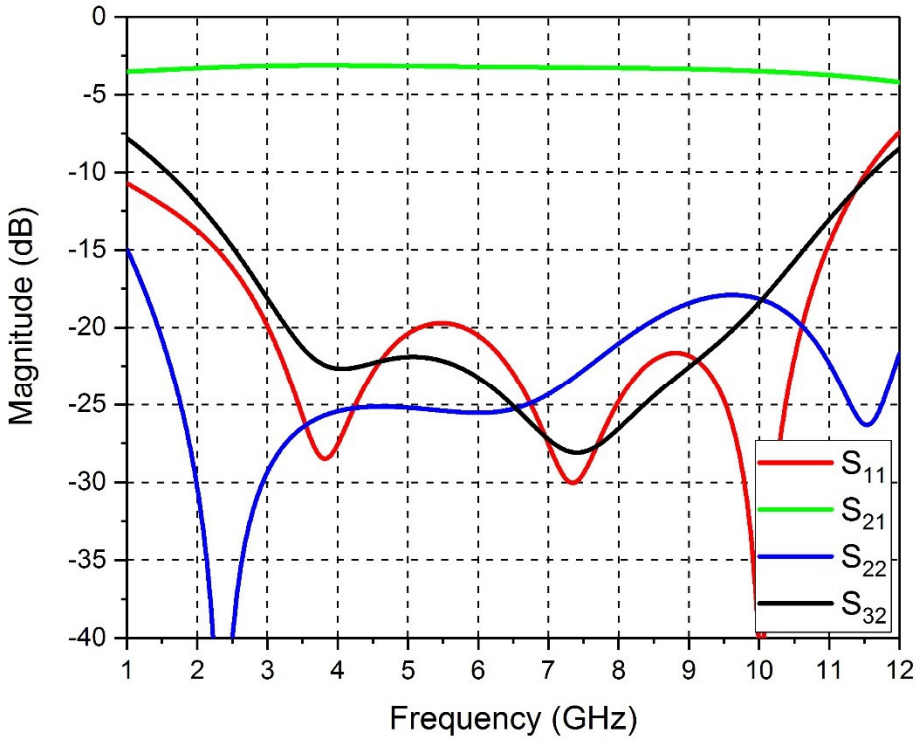


Figure 3.18. The S-parameters for the optimised miniature two ports UWB power divider.

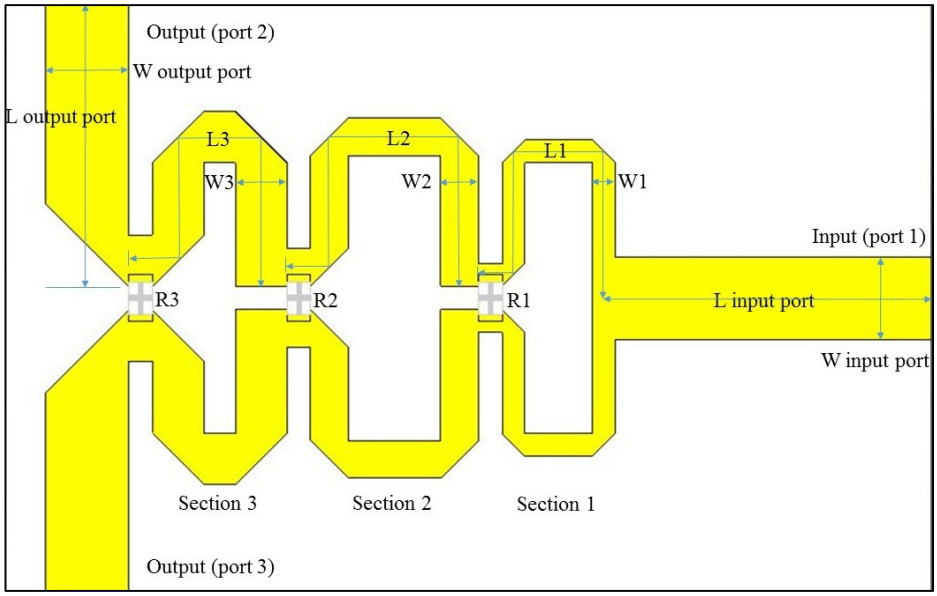


Figure 3.19. The miniature two ports UWB power divider layout.

To construct a four ports power divider, three of the two ports power dividers are used. Two staged power divider is constructed by connecting the output port of the first stage to the input port of the second stage, which consisted of two power dividers. The 50 Ω output ports of the first stage have been extended to connect the input ports of the second stage as shown in Figure 3.20. The impedance value of the first stage output ports is fixed, even after extending them, as the impedance is a function of the microstrip width according to equations (3.2) and (3.9) for a given substrate permittivity, thickness and copper thickness. The initial simulated S-parameters are shown in Figure 3.21. Optimising the structure enhanced the return loss as shown in Figure 3.22.

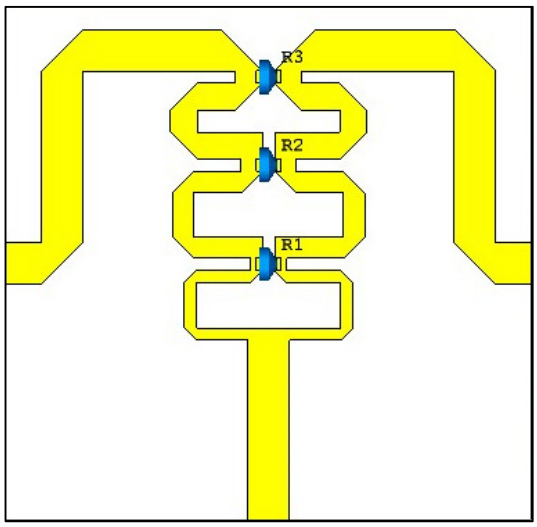


Figure 3.20. Extended output ports 1 to 2 UWB power divider.

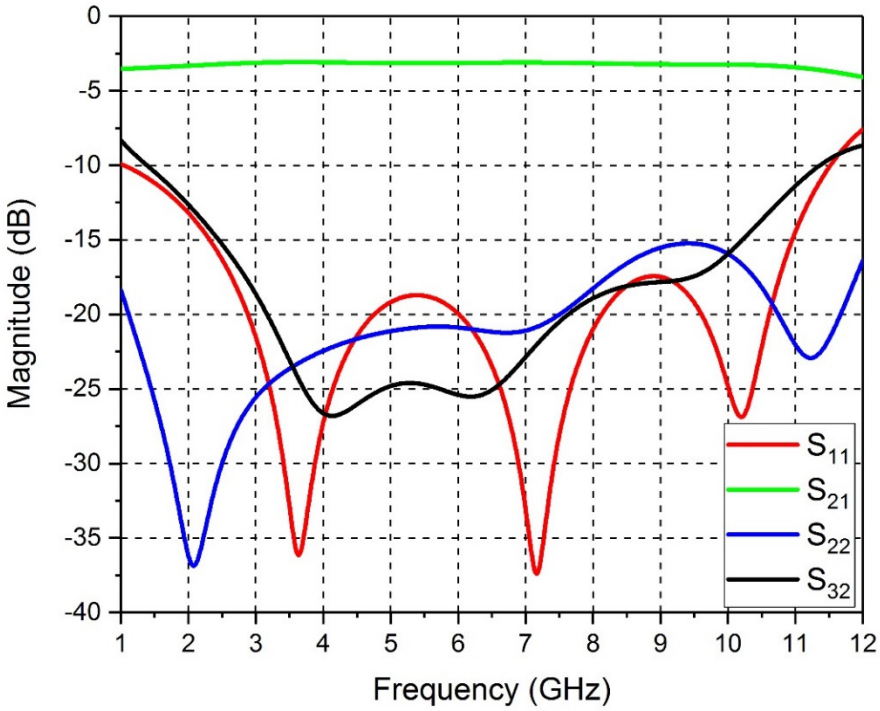


Figure 3.21. The initial simulated S-parameters for the extended output ports of the miniature UWB power divider.

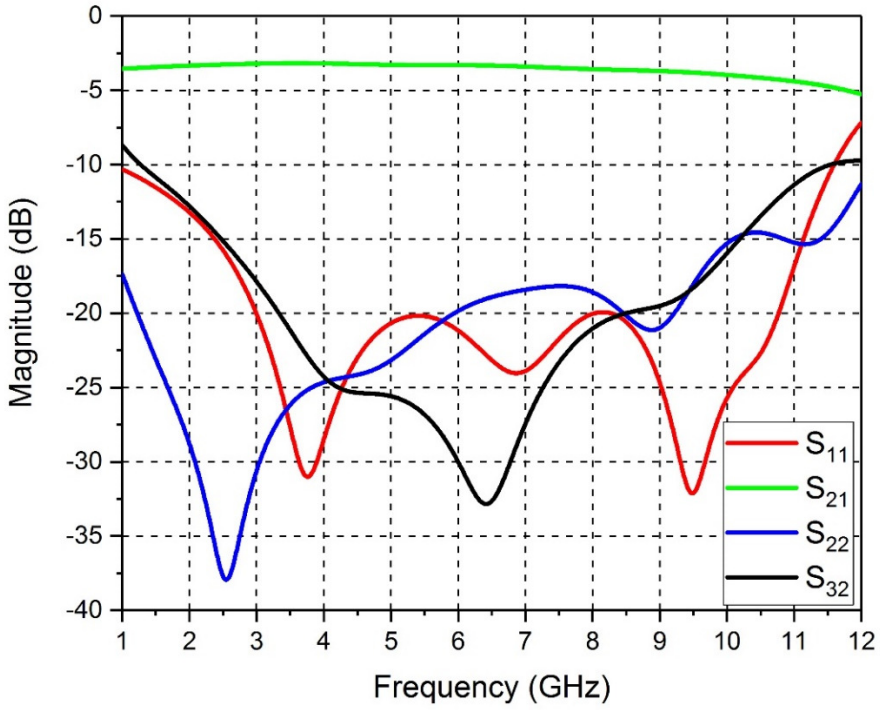


Figure 3.22. The S-parameters for the optimised extended output ports of the miniature UWB power divider.

The S-parameters for the four ports power divider are shown in Figure 3.23, which clearly shows that the optimised return loss is equal to or better than 20 dB for the required band. A 6.5 dB insertion loss and 16 dB isolation are achieved. The overall optimised board dimension is 60.16 mm × 19.94 mm.

Table 3.6 presents a comparison between the proposed two ports UWB power divider and similar power dividers in published works [3-7, 62-65]. The table shows that the proposed power divider is comparable in size to the power divider reported in [3] but the proposed power divider is better in performance in terms of the achieved return losses.

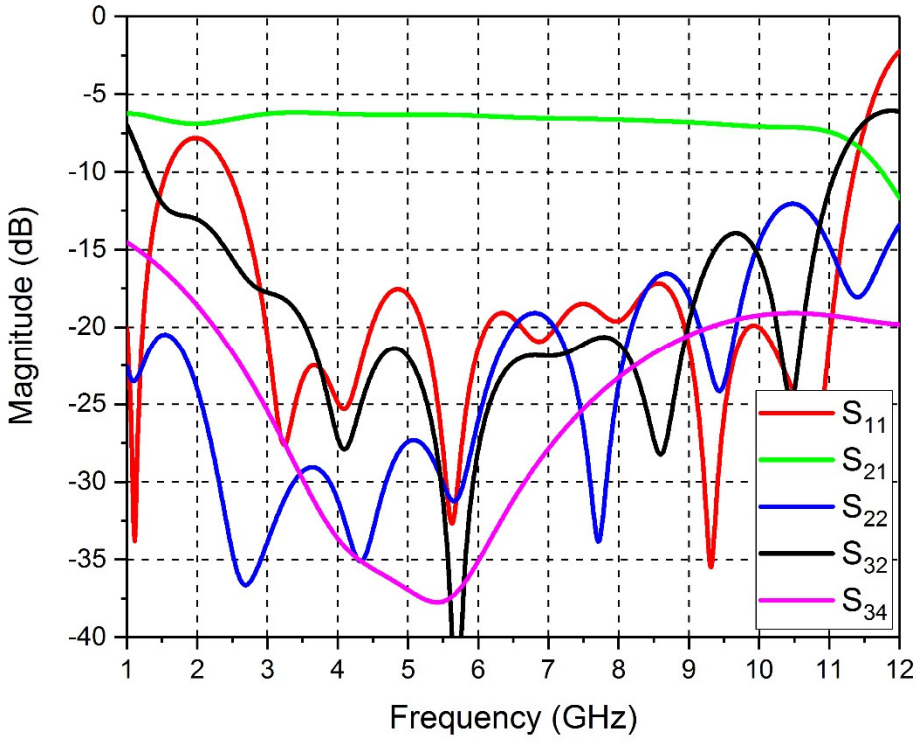


Figure 3.23. The optimised S-parameters for the miniature 1 to 4 UWB power divider.

A thin film 100 Ω surface mount resistor (SMD) terminates the first and the second sections, while a 422 Ω SMD resistor terminates the third section. A '0402' package size SMD resistor was used with a footprint of 1 mm × 0.5 mm. The fabricated two and four ports power dividers are shown in Figure 3.24 and Figure 3.25 respectively. The measured S-parameters are shown in Figure 3.26 and Figure 3.27 for the two and four ports UWB power dividers. A 10.5 and 8.25 GHz operational bandwidth for return loss better than 10 dB is achieved for the two and four ports power divider respectively. The measured and simulated insertion losses are consistent in the realized bandwidths, namely 3 ± 0.2 dB and 6 ± 0.13 dB for the two and four ports power dividers respectively. The difference between the measurements and simulation could be due to fabrication imperfection and the soldering amount besides SMD resistor positioning.

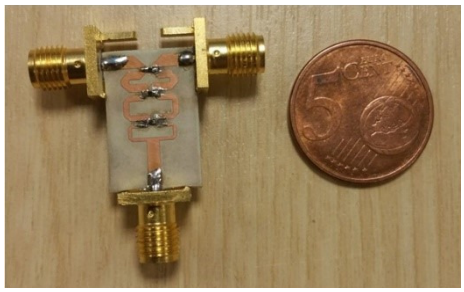


Figure 3.24. Fabricated board for the 1-2 ports UWB power divider.

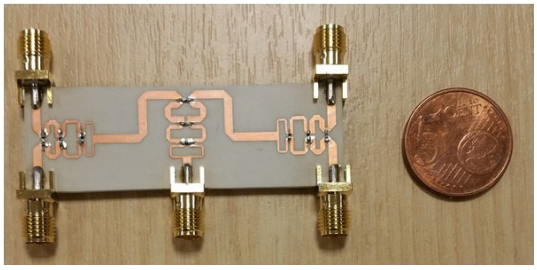


Figure 3.25. Fabricated board for the 1-4 ports UWB power divider.

Table 3.6. Comparison of the presented 1-2 UWB power divider with previous works.

Reference Number		S_{11} (dB)	S_{21} (dB)	S_{32} (dB)	Size (mm× mm)
[3]	simulation	-11	-3	-20	13×18
	measurement	-11	-3	-16	
[4]	simulation	-13	-3.2	-11	16×32
	measurement	-12	-3.15	-9	
[5]	simulation	-12	-3.15	-10	16×18
	measurement	-14	-3.3	-10	
[6]	simulation	N/A	N/A	N/A	20×11.5
	measurement	-15	-3	-10	
[7]	simulation	-11	-3.5	-7.5	20×30
	measurement	-15	-3.52	-15	
[62]	simulation	N/A	N/A	N/A	13×32
	measurement	-10	-3.5	-10	
[63]	simulation	-10	-3.3	-13	21×34
	measurement	-12	-3.3	-15	
[64]	simulation	-13.5	-2.8	-7.5	15.5×22
	measurement	-11	-3.5	-14	
[65]	simulation	-11	-3.5	-10	16×17
	measurement	-11	-3.5	-10	
Presented work	simulation	-20	-3	-17	13×19.5
	measurement	-16	-3	-12	

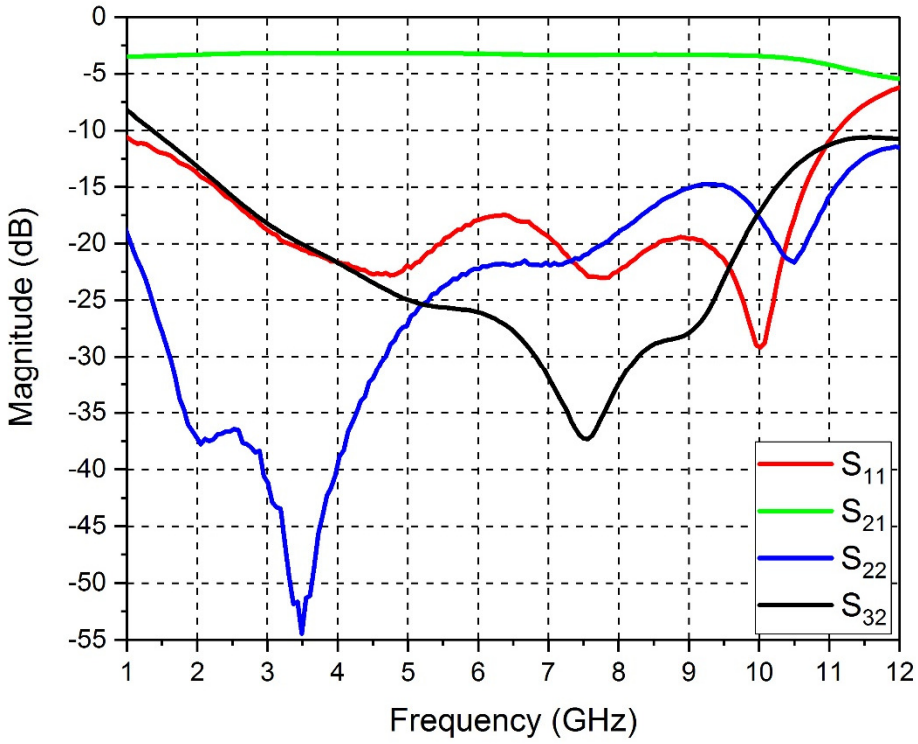


Figure 3.26. Measured S-parameters for the two ports UWB power divider.

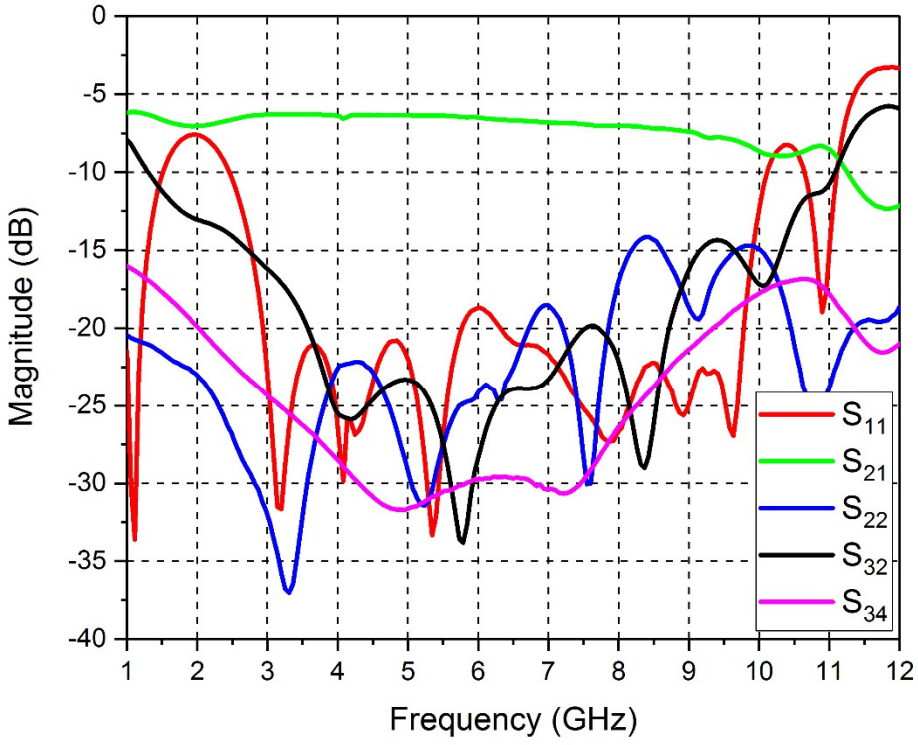


Figure 3.27. Measured S-parameters for the four ports UWB power divider.

3.2 Multi-Output Ports Power Divider

This section is based on an under review paper [66], in this section, a novel general design for microstrip-fed multi-output ports planar Wilkinson power divider is proposed, designed and fabricated for industrial, scientific and medical radio band applications. The proposed power divider operates in a wideband frequency range that is from 1.77 to 2.88 GHz with a low insertion loss imbalance, which is below 0.01 dB at 2.4 GHz. The presented design has a simple structure utilize a microstrip feeding port. The power divider adopts a two-layered substrate structure solving isolation resistor interconnection crossover problem for dividers having more than two output ports. A one-section quarter wave transformer is employed on the upper layer and the third layer is used to interconnect isolation resistors between output ports. Two different permittivity substrates are selected to simplify the design structure. A prototype of one to five ports power divider is selected as a design example and fabricated. The measured S-parameters are well agreed with the simulation, which validates the design concept.

The block diagram for a general one to N output ports Wilkinson power divider is shown in Figure 2.9, where N is the number of output ports. It shows the isolation resistors are connected in a star configuration. Power dividers with two output ports do not suffer from a problem in connecting the isolation resistor, as only one is needed. The quarter wave transformers are separated with a small spacing, which is usually kept as a fraction of the operational wavelength to ensure better input and output ports return loss and output ports isolation. Transmission lines are having a λ/2 periodicity phenomenon. So that the same impedance can be transformed every λ/2 [2]. Thus, a line with a length of λ/2 and its multiplication

can be used to connect isolation resistors between separated output ports. Three power dividers are designed with a different layout for the isolation resistors interconnection microstrip line to verify that the λ/2 added length for the isolation resistor interconnection line and its place does not affect to power divider performance.

The first power divider is a uniplanar structure and each isolation resistor interconnection microstrip line has a length of λ/2 that is implemented on the same layer of the power divider as shown in Figure 3.28. The S-parameters for the input port and one of the output ports are shown in Figure 3.29 to simplify the plots. The minimum achieved input port return loss is 33.08 dB at 2.36 GHz. The corresponding output port return loss, insertion loss and isolation is 33.51, 3.1 and 38.03 dB respectively at the same frequency. The power divider has an operational bandwidth of 1.28 GHz from 1.74 to 3.02 GHz where input and output port return losses and isolation are better than 10 dB.

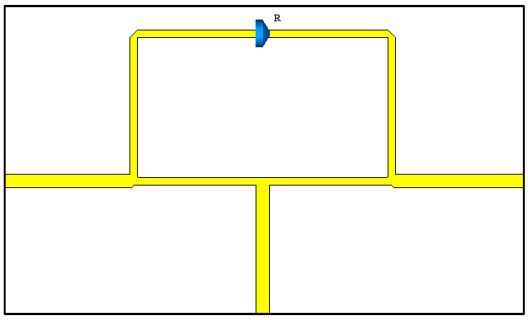


Figure 3.28. The structure of the uniplanar power divider that has an extended isolation resistor interconnection microstrip line on the same layer.

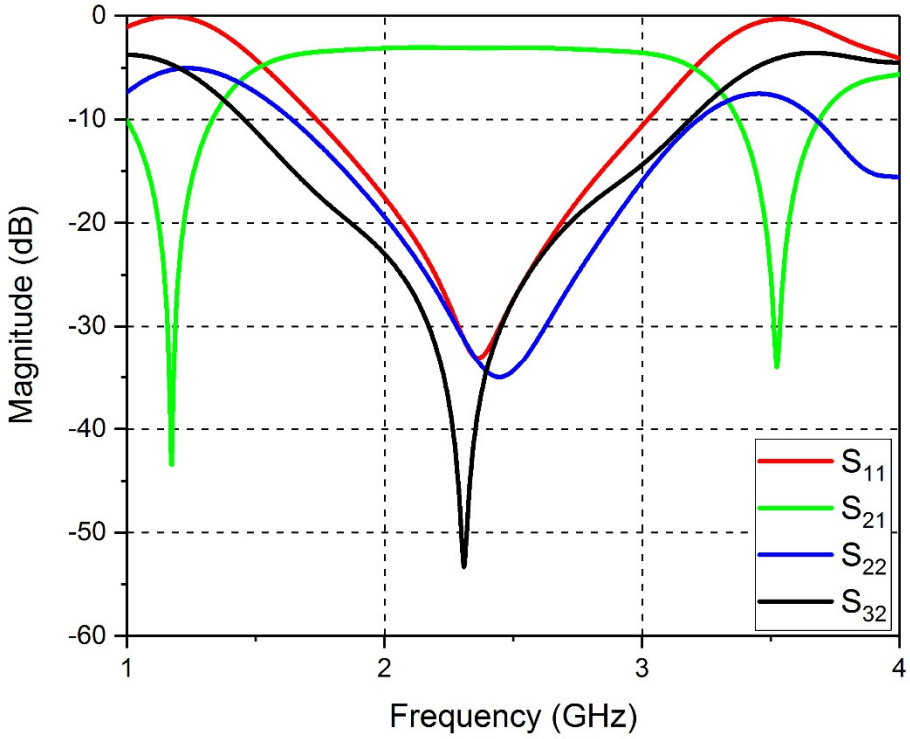
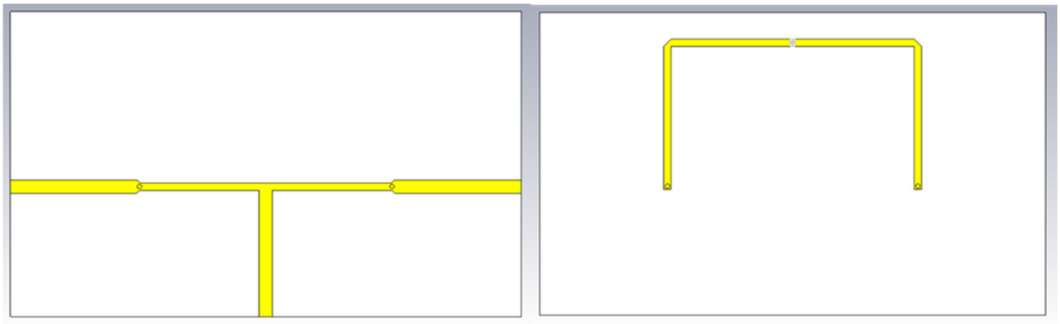


Figure 3.29. The simulated S-parameters of the uniplanar power divider that has an extended isolation resistor interconnection microstrip line on the same layer.

The second power divider is designed in a way so that the isolation resistor interconnection microstrip line is implemented on another layer beneath the ground layer of the power divider as shown in Figure 3.30. The isolation resistor interconnection microstrip lines are connected using two vias to the upper layer at the point where the end of the quarter wave transformer connects with the output port.



(a) (b)

Figure 3.30. The double layered power divider. (a) The upper power divider layer showing the quarter wave transforms. (b) The lower layer showing the isolation interconnection microstrip lines.

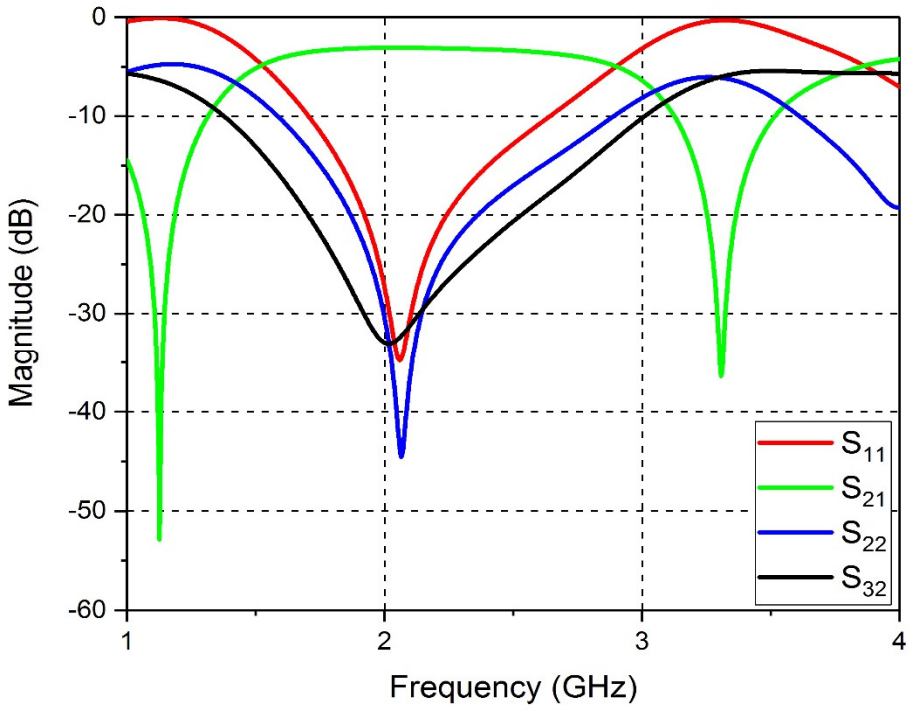


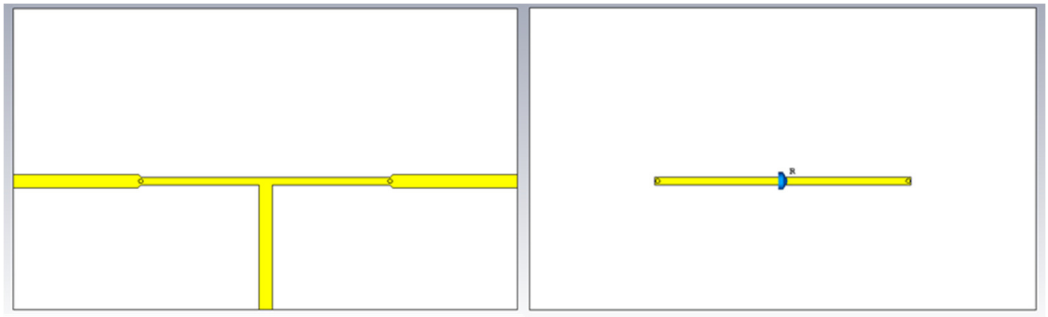
Figure 3.31. The simulated S-parameters of the double layered power divider.

The minimum achieved input port return loss is 34.79 dB at 2.06 GHz. A 300 MHz frequency shifting is observed, this is due to introducing additional reactance by using vias to connect the isolation resistors microstrip lines with the upper layer. To shift the minimum of the return loss to a higher frequency, the length of the

quarter wave transformer can be shortened. The simulated output ports return loss, insertion loss and isolation is 43.6, 3.07 and 32.45 dB respectively. The operational bandwidth of this power divider is 930 MHz from 1.71 to 2.64 GHz.

The third power divider is designed using the same parameters as the previous design but the isolation resistor interconnection line is designed to be a straight line. To achieve that, the upper layer substrate dielectric constant selected to be lower than the dielectric constant of the lower layer substrate. So that, the total physical length for both isolation resistor interconnection line and substrate thicknesses is equal the half-electric wavelength, which is equal to the physical length of the quarter wave transformer. This method allows constructing a short microstrip line for the isolation resistor interconnection as shown in Figure 3.32 (b).

The simulated S-parameters are shown in Figure 3.33 for the triple-layered power divider that has a short isolation resistor microstrip line length. The minimum input port return loss is measured at 2.14GHz and it is 37.46 dB. While output ports return loss, insertion loss and isolation are 49.60 dB, 3.1 dB, 39.18 dB respectively. The operational bandwidth is 680MHz from 1.87 to 2.55 GHz.



(a) (b)

Figure 3.32. The double layered power divider with straight isolation resistor interconnection line. (a) The upper power divider layer showing the quarter wave transforms. (b) The lower layer showing the short straight isolation interconnection microstrip lines.

By comparing the results of the three different structures, it is clear that the performance of all power dividers is almost the same as the input and output ports return loss and the isolation is below 30 dB at the minimum simulated input return loss. Besides that, the insertion loss for all of them is about 3.1 dB. The only difference is that the first design has a wider bandwidth of 1.28 GHz while the second design has a 930 MHz bandwidth and the third design has a bandwidth of a 680 MHz. This can be solved by optimising the power divider parameters, in return, the problem of isolation resistor crossovers can be solved using the third technique.

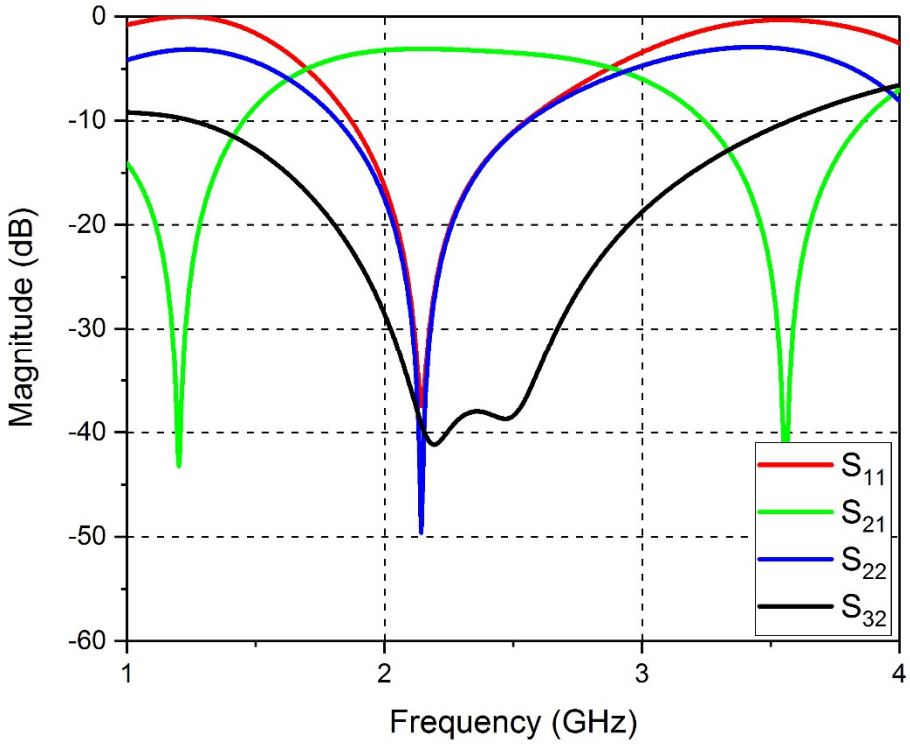


Figure 3.33. The S-parameters of the double layered power divider with straight isolation resistor interconnection lines.

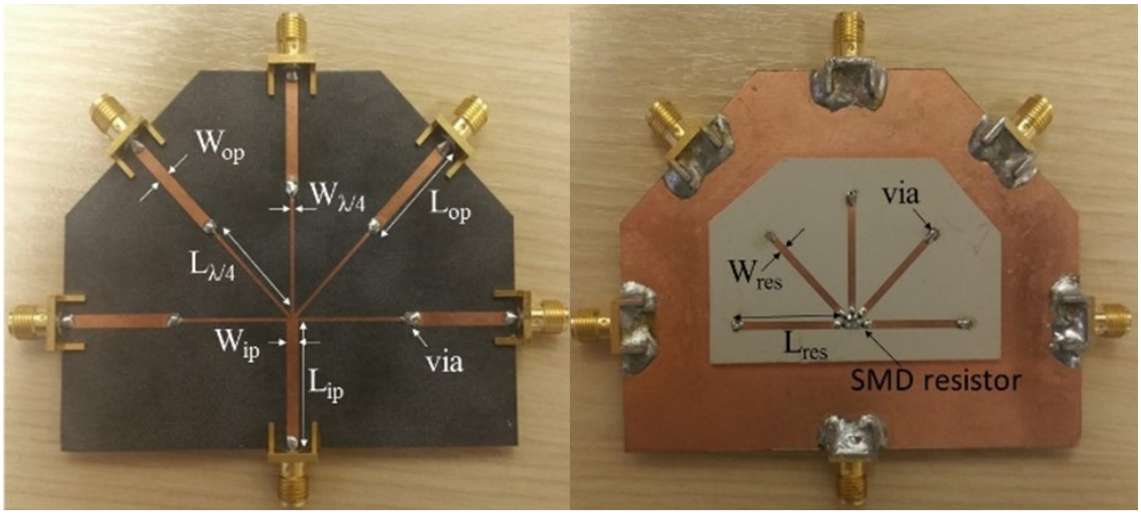
In order to achieve a single section planar power divider with output ports more than two, the multi-layered substrate is used. The input and output ports with quarter wave transformers designed to be on the upper layer, whilst the resistors with their interconnection microstrip lines implemented on the lower layer as shown in Figure 3.30 and Figure 3.32. These two layers are separated with common ground and vias used to connect resistor section with the intersection point of the quarter wave transformer and output ports.

To prove the concept, a five-output ports power divider was designed and the values for $Z_{N/2}$ and the SMD resistor (R) are found to be 111.8 Ω and 50 Ω respectively using equation (2.36) and equation (2.37). The optimised values for

the design parameters are listed in Table 3.7, which are approximately calculated by using equations (3.1) to equation (3.5) that are optimised to obtain the best performance. The proposed planar Wilkinson power divider is shown in Figure 3.34. The first layer implemented on a 0.51mm thick Rogers RO5880 substrate with a dielectric constant of 2.2 and the bottom layer implemented on a 1.28 mm thick Rogers RO3010 substrate with a dielectric constant of 10.2. Arbitrary impedance can be selected for the isolation resistor interconnection microstrip lines, as its impedance does not effect on the results, which has been validated by a parametric study.

Table 3.7. The proposed power divider design parameters.

	Impedance (Ω)	Length (mm)	Width (mm)
Input port	50	23.73	1.45
λ/4 section	111.8	25.27	0.378
Output ports	50	22.78	1.78
Resistors interconnection	arbitrary	25.27	1



(a) (b)

Figure 3.34. The fabricated proposed power divider photograph. (a) The upper layer showing input and output ports with the quarter wave transformers. (b) The lower layer sowing isolation resistors and its microstrip line interconnections.

Although a similar concept has been reported in [10], in that work, a more complicated design was needed and a complex fabrication procedure was used. A coaxial feeding port was used that was soldered on the ground layer, which was between the two substrates that lead to the need of drilling the central part of the lower layer to allow placing the coaxial connector. In contrast to that, difficult to implement a feeding method, a microstrip line is used in this design, which made it more suitable for planar structure applications. In addition, an impedance matching disk was required in the previous work to feed the quarter wave transformer sections to obtain a better input port matching, while the quarter wave transformer sections are directly connected to the input port without the need to an additional structure to be introduced in the proposed design. That helps to reduce the required number of drilled via holes in the proposed power divider. Moreover, an Archimedean spiral line was needed for the isolation

resistor interconnection in [10], which required additional calculations. While a straight microstrip line is used benefiting from implementing the isolation resistors microstrip line interconnection on a high permittivity substrate in the proposed power divider. In addition, the reported work placed a microstrip ring on the lower layer around the coaxial connector, which was needed for interconnecting isolation resistors due to placing the SMA connector in the middle of the structure. While in the presented work, isolation resistors are connected directly without the need for additional structures. In [10], the same concept of [67] was used but implemented for dual-band operation.

The simulated and measured S-parameters for the fabricated power divider are shown in Figure 3.35. It is clear that the power divider covers a wide bandwidth of 1.11 GHz from 1.77 to 2.88 GHz with a return loss of 25.5 dB at 2.4 GHz and maintaining the return loss better than 10 dB all over the operational band. All output ports return losses are about 18 dB at 2.4 GHz and they are better than 15 dB for the operational band. The isolation performance between output ports is around 25 dB at 2.4 GHz with maintaining it better than 20 dB all over the band as shown in Figure 3.36. The measured insertion loss at 2.4 GHz is 7.4 dB compared to 6.99 dB theoretical value. The amplitude imbalance is less than 0.01 dB at 2.4 GHz as shown in Figure 3.37. In order to simplify the plots, only three ports are selected, which are the input port (port one) and two output ports (ports two and three) to show the power divider performance and compare the measurements with the simulation.

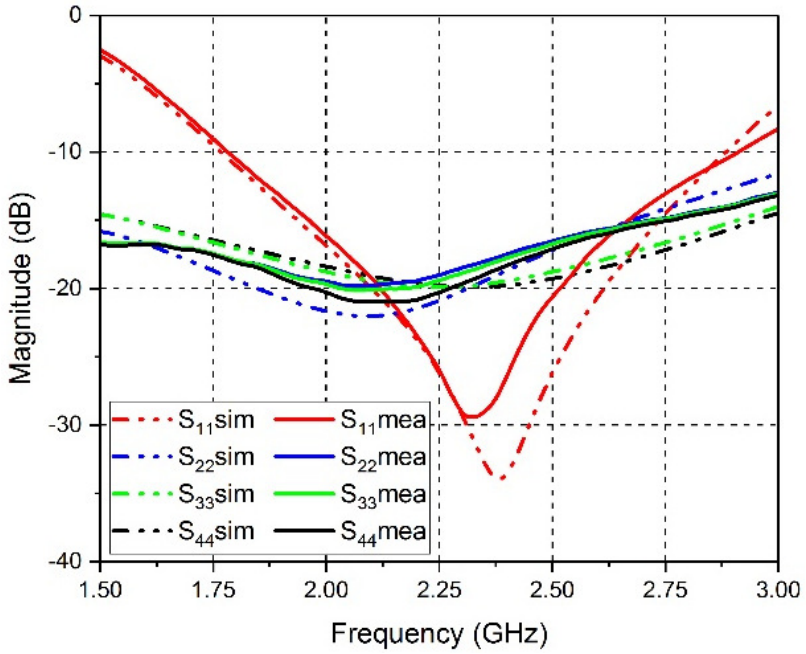


Figure 3.35. The simulated and measured input and output ports S-parameters.

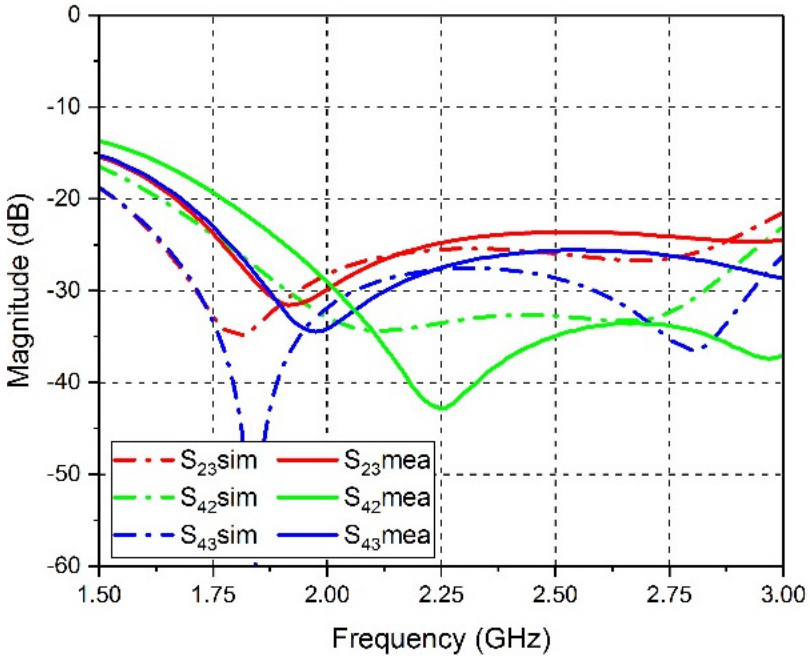


Figure 3.36. The simulated and measured output ports isolation.

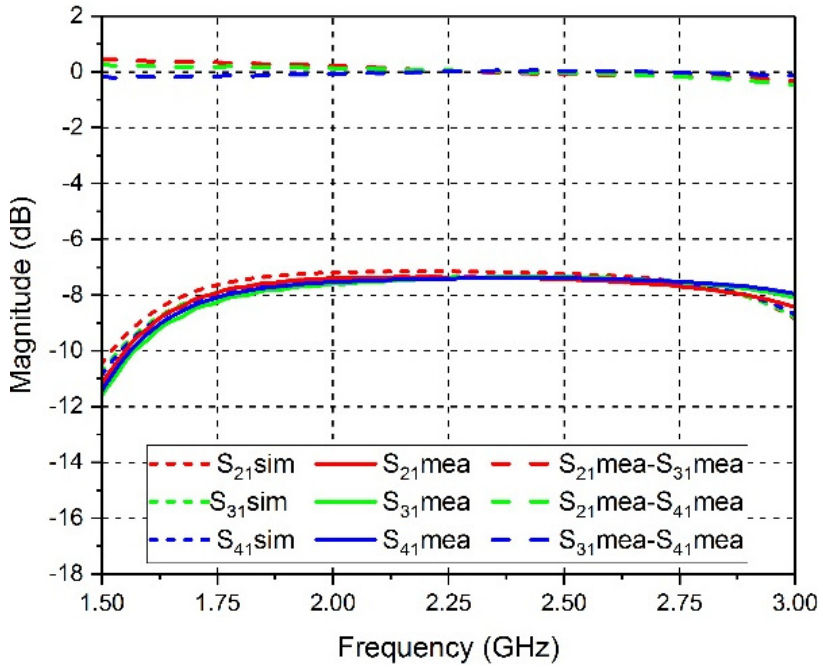


Figure 3.37. The simulated and measured insertion loss with measured output ports imbalance.

Two parametric studies are carried out to study the effect of changing the width of the isolation resistor interconnection microstrip lines and the diameter of the via on the power divider performance to find the optimum width and diameter for the proposed design. A range from 0.8 to 1.2 mm is selected for the microstrip line width with an increment step of 0.2 mm. Figure 3.38 shows the power divider performance for each case. It is clear that the isolation resistor interconnection microstrip lines width does not have a noticeable effect on the performance, although, the input and output ports return loss and the isolation between output ports are slightly changed but that can be neglected. For that reason, an arbitrary width is selected, which is 1 mm to facilitate the soldering of the SMD resistors.

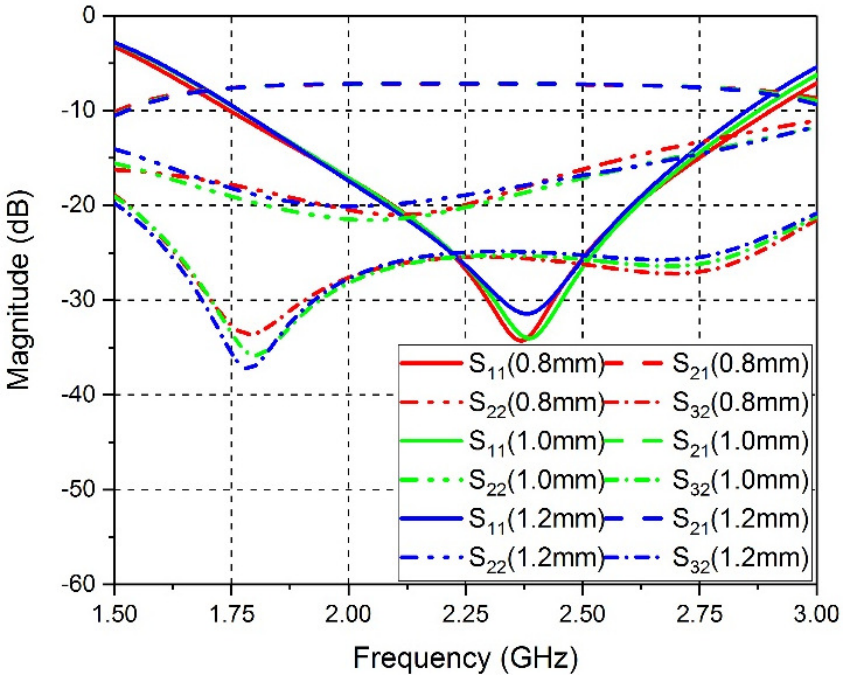


Figure 3.38. The power divider S-parameters performance with different isolation resistors interconnection microstrip line widths.

Similar behaviour for the power divider performance can be observed from Figure 3.39 when changing via diameters from 0.8 to 1.2 mm with an increment of 0.2 mm. It can be observed that the diameter of the via does not effect on the power divider performance. However, a 0.8 mm vias diameter is selected in this design.

The power divider performance is not affected by changing isolation resistors interconnection microstrip line widths and via diameters due to the symmetry of the structure. As the reflected signal from output ports going through the isolation resistors is propagating through a similar path so that any loading due to changing the path impedance or additional capacitances added due to using vias is applied identically to all other paths in which the effect is cancelled each other.

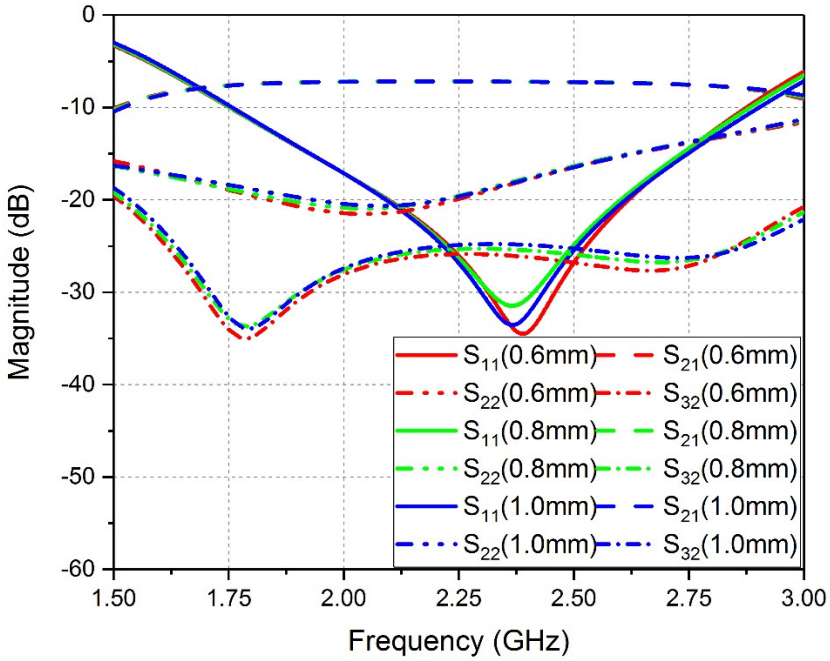


Figure 3.39. The power divider S-parameters performance with different via diameters.

3.3 Reconfigurable Output Power Wilkinson Power Divider

This section is based on an published paper [68]. The aim of this section is to present the design of a novel reconfigurable Wilkinson power divider with equal to 8 dB power difference between output ports using one varactor diode.

The proposed power divider adopts the microstrip coupled line technique to implement a high impedance quarter wave transformer section to have an unequal output power values. A varactor diode is placed between the coupled line to achieve reconfigurability by changing the reverse biasing voltage on the varactor diode. This enables equal to 8 dB power difference between output ports. A wide range of biasing voltage is used to achieve a smooth control on output ports power difference. Prototype hardware is fabricated and measured to

validate the proposed approach. In the equal output power scenario, the measured performance shows a bandwidth of 550 MHz at 5.4 GHz. A higher bandwidth of 750 MHz and 1 GHz is obtained in the case of 6 dB and 8 dB output ports power difference scenarios.

To achieve high power division ratio, several novel techniques were presented to realise high impedance microstrip transmission lines. One of these methods implemented a defected ground structure (DGS) microstrip line [14-18]. In which a conventional Wilkinson power divider was used but the ground plane under one of the quarter wave transformers was defected by a rectangular shape. The defect in the ground under the microstrip line adds an additional inductive component to the microstrip line to be able to realize very high impedance of 150 Ω and over. The DGS increased the characteristic impedance of the microstrip line to be much higher than that of a conventional microstrip line without the DGS for the same microstrip width. Besides that, the equivalent microstrip line was shorter in length. However, the drawback of using the DGS is that the ground layer is very sensitive to metallic enclosures and conductors [19]. A solution is reported in [69] in which the authors introduced an additional ground to solve this problem. The second method to achieve high power division ratio is by using a coplanar waveguide with electromagnetic band gap (EBG) [19, 20], in which narrow slots were etched in the coplanar structure to obtain a high impedance transmission line. Another method to implement a high impedance microstrip line is by offsetting double-sided parallel strip lines [21]. This technique considered to be easier to implement compared to the DGS technique as this allowed some design freedom as claimed in [70, 71]. The high impedance is realised by

increasing the distance of the offset or by decreasing the strip line width, which deteriorates the power handling. In [22], applying groove alongside a microstrip line is used to achieve the high impedance section. This technique needed an additional fabrication processes for properly applying the grove with accuracy limitations. In [72], the high power division ratio was achieved by cascading low ratio divider. In the same reference, doubling the substrate thickness with an air gap allowed implementing a high impedance section. Loading a transmission line with open and short stubs was another technique to implement a high impedance section [73, 74]. Using a coupled microstrip line was reported in [75]. In this method, the high impedance section was implemented by coupled line and terminating their ends to the ground. Conversely, such as in [76], the low impedance transmission line was loaded with periodic shunt open stub to achieve very low impedance line. Also in [77], the low impedance transmission line was modified by employing a dual transmission line with a different length that was used to implement an extremely unequal Wilkinson power divider.

None of the mentioned works achieved a continuous power division ratio except in [16, 17] where two varactor diodes were placed between the ground plane and a floating potential conductor under the high impedance line claiming to have a tuneable division ratio. However, the drawback of using DGS is that the ground plane should be kept far from any other electromagnetic materials [19], as the defected ground considered as a high radiating structure that is affected by other adjacent material.

In this section, a parallel microstrip coupled line technique is utilized to design a high impedance quarter-wave transformer Wilkinson power divider with terminating the open ends of the coupled line to the ground. To obtain the reconfigurability feature, one varactor diode is needed that is placed at the mid-distance between the coupled line ends.

A 3:1 unequal Wilkinson power divider ration is designed using the coupled line technique. Figure 3.40 shows the schematic diagram of the proposed power divider. The characteristic impedance for the power divider sections, shown in Table 3.8, are calculated using equations (2.39) to equation (2.43).

Table 3.8. The calculated design parameters for the proposed power divider.

	Value (Ω)	Width (mm)	Length (mm)
Input / output ports	50	1.84	8.47
Z11	43.9	2.26	25.18
Z12	28.9	4.1	8.16
Z21	131.6	0.125	9.31
Z22	86.6	0.63	8.84

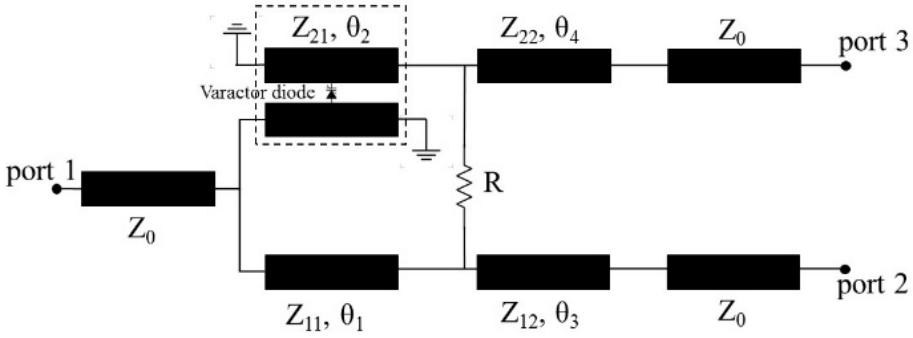


Figure 3.40. The schematic diagram of the proposed power divider.

The electrical length for θ_2, θ_3 and θ_4 are designed to be quarter wavelength. The quarter wavelength coupled line, which there ends are grounded that shown in Figure 3.40, resulting in an extra 180° phase shift to the signal passing through it [75]. Therefore, the electrical length of θ_1 is designed to be three-quarter wavelength to compensate the 180° phase shift passing in the other branch. The calculated isolation resistor (R) is 115.5 Ω according to equation (2.41). The nearest available off shelf resistor is used, in this case, it is 115 Ω. The microstrip lines physical dimensions are calculated using equations (3.2) to equation (3.5). The coupled line dimensions are calculated using Agilent ADS Line calculator. The proposed power divider design dimensions are listed in Table 3.8.

The high impedance section Z_{21} is constructed by using a microstrip coupled line structure with a coupling factor of 0.3 [75] and terminating the open ends to the ground. The calculated gap between the coupled line is 0.49 mm. A varactor is added that acts as a variable capacitance between the coupled line to achieve the low odd-mode impedance needed for tight coupling [78]. According to that, the coupled line width and the gap between them are re-calculated taking into

consideration the varactor existence. The new width and gap between the coupled line (WZ_{21}) are 0.4 and 0.108 mm respectively.

Rogers RO4003C substrate with dielectric constant of 3.38 and a thickness of 0.813 mm is used to fabricate the proposed power divider. Figure 3.41 shows a photograph of the fabricated power divider with an overall dimension of 50 mm × 40 mm. Capacitors of 850 pf are placed on the input and the output ports to isolate the DC biasing voltage of the varactor diode from the vector network analyser. An inductor of 96 nH is used to isolate the RF signal from returning to the DC source. A silicon junction varactor diode from Skyworks (SMV1231) is used between the coupled line. Changing the reverse biasing voltage of the varactor diode from 0 to 15 V changes the equivalent capacitance of the varactor diode from 0.4 to 2.1 pf. This corresponds to an output power difference ranging from 8.25 to -1.15 dB, as shown in Figure 3.42.

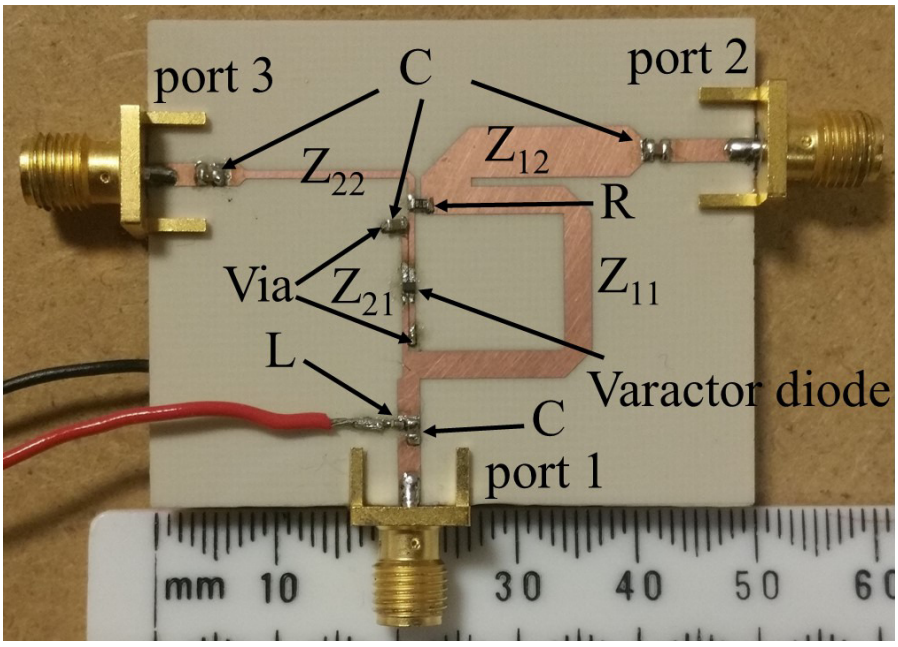


Figure 3.41. A photograph of the fabricated reconfigurable power divider.

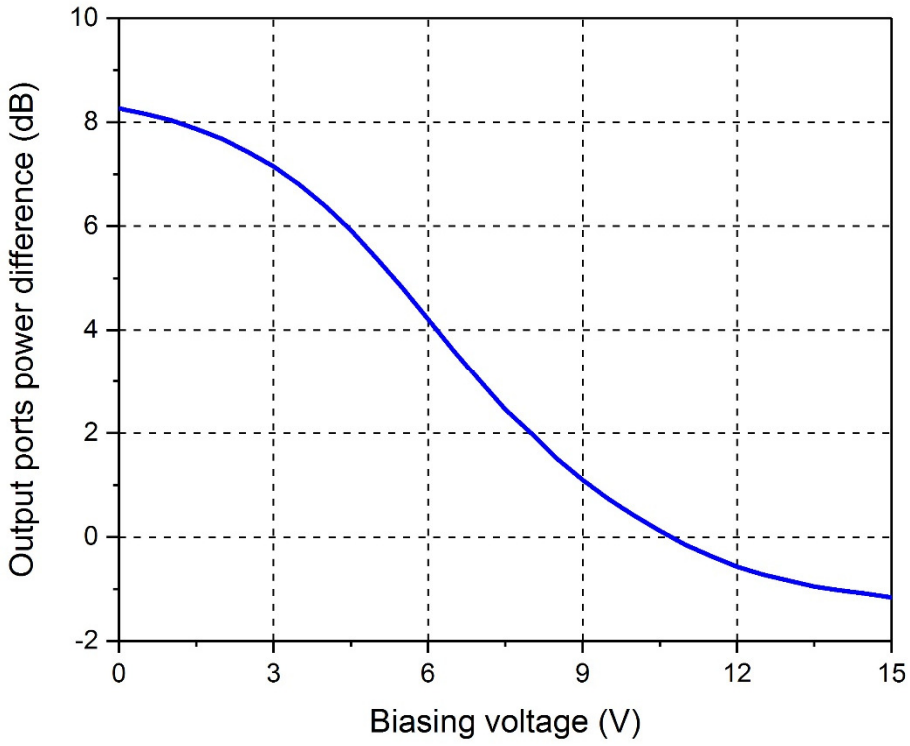


Figure 3.42. The measured response with reverse biasing voltage.

The proposed unequal power divider is designed to work at 5.5 GHz for WLAN applications. The measured performance shows a 6 dB output power difference as shown in Figure 3.43. To achieve this power difference, a 4.4 V reverse biasing voltage is applied across the varactor diode. The input port return loss is better than 10 dB for a bandwidth of 750 MHz ranging from 5 to 5.75 GHz and the insertion loss of port 2 and 3 is 5.6 and 11.8 dB respectively at 5.5 GHz, which validates the 6 dB output ports power difference. The amplitude imbalance for 40 MHz WLAN channels within the operational band of 750 MHz is bellow ± 0.1 dB.

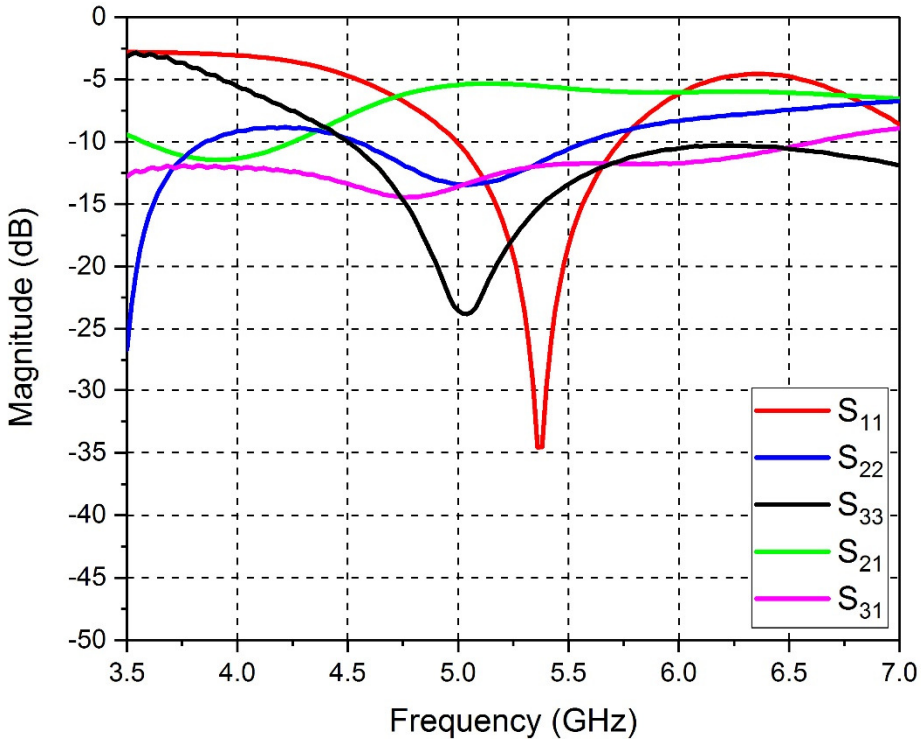


Figure 3.43. The measured S-parameters of the proposed reconfigurable power divider for 6 dB output ports power difference scenario.

A 1 V reverse biasing voltage is applied across the varactor diode to achieve an 8 dB output ports power difference. The S-parameters for this case are shown in Figure 3.44. The input port return loss bandwidth is 1 GHz from 4.75 to 5.75 GHz. The insertion loss of ports 2 and 3 is 5.6 and 13.5 dB respectively at 5.5 GHz. The amplitude imbalance for the 40 MHz WLAN channels is also bellow ± 0.1 dB.

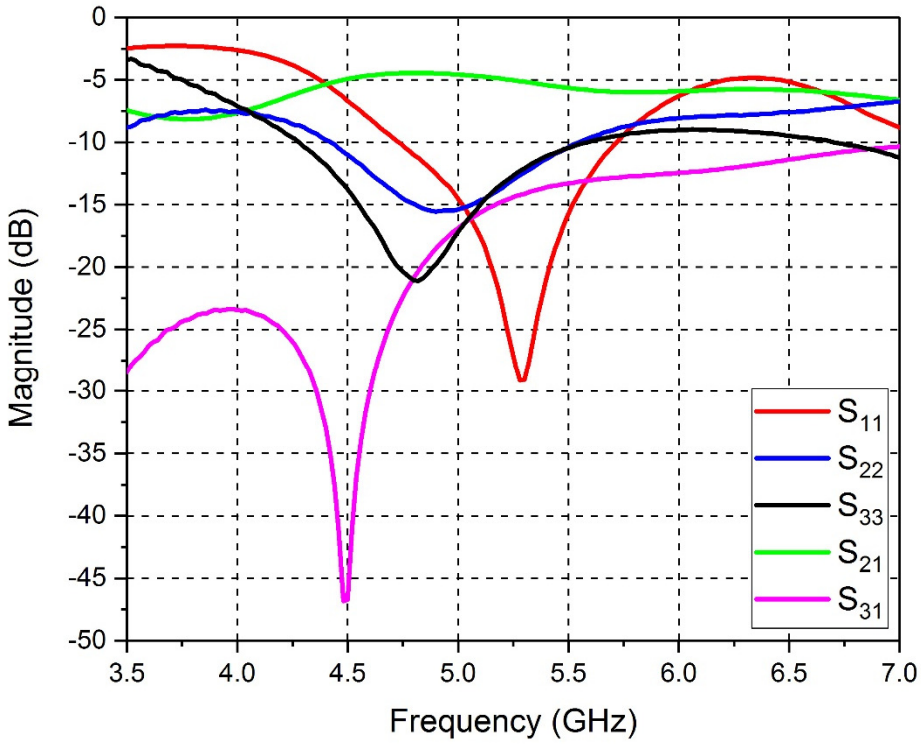


Figure 3.44. The measured S-parameters of the proposed reconfigurable power divider for 8 dB output ports power difference scenario.

For equal division ratio scenario, a 10.4 V reverse biasing voltage is applied. Figure 3.45 shows that the return loss is better than 10 dB for a bandwidth of 550 MHz from 5.2 to 5.75 GHz. It is clear that both output ports have an equal insertion loss of 6.7 dB at 5.5 GHz. The amplitude imbalance in this case for the 40 MHz WLAN channels is bellow ± 0.2 dB. Figure 3.42 shows that the proposed power divider has a wide control range of 9.4 volts, which helps to achieve more precise output ports power difference using a single varactor diode for every 5 GHz WLAN channels.

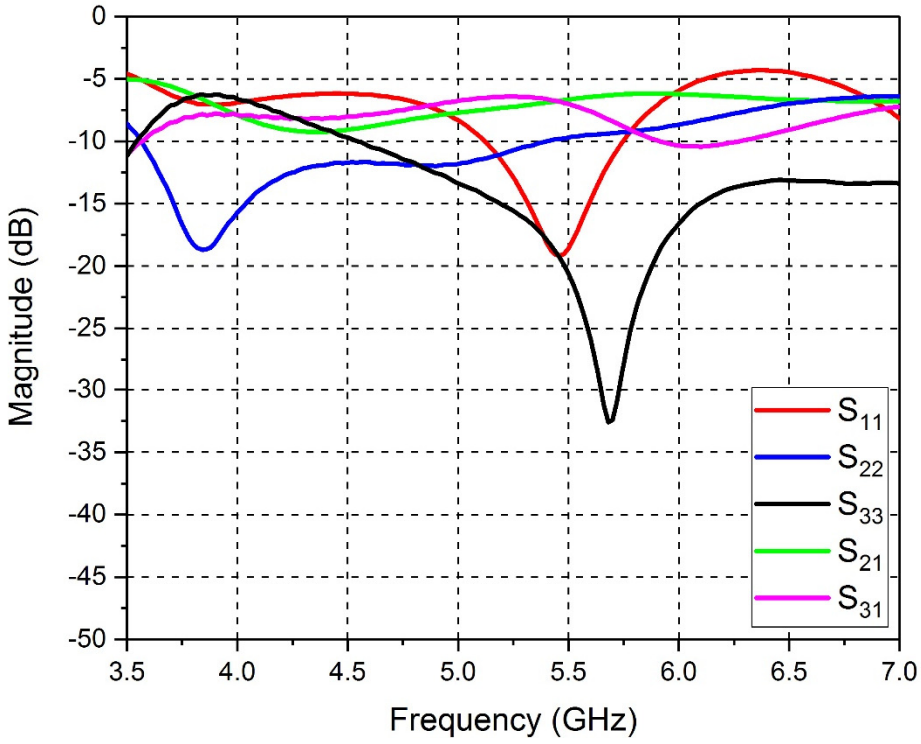


Figure 3.45. Measured S-parameter of the proposed reconfigurable power divider for equal output ports power scenario.

3.4 Summary

In this chapter, various configurations of Wilkinson power dividers were studied, designed and fabricated. An important size deduction achieved by selecting a compact structure and substrate permittivity. A multiple section method was used to design the 1 to 4 UWB power divider (3.1 to 10.6 GHz). The small size designs for both 1 to 2 and 1 to 4 dividers made them suitable for applications where size and performance are critical, such as mobile devices and antenna array feeding networks.

The five-way planar power divider proposed a solution to overcame the isolation resistor interconnection crossover problem for multi-output ports power dividers

by introducing a third layer. The simple design structure made the fabrication procedure much easier compared to previous works.

The proposed reconfigurable power divider was capable to deliver equal and up to 8 dB output ports power difference between the output ports using only one varactor diode and applying a wide range of reverse biasing voltage that helped to control the power difference more accurately compared to previous works.

The simulation and experimental results for all designs were largely agreed, which validated the design approaches. The resultant power divider designs in this chapter were adopted in the fifth chapter where antenna array configurations have been applied.

Chapter 4

Practical Antenna Designs

With the rapid development of wireless technology innovation, compact size, low profile, lightweight, wideband, and multiple functional antenna designs are becoming more attractive in many microwave applications. In this section, different patch antenna structures are investigated in order to fulfil these requirements. As patch antennas demonstrate many advantages, including simple fabrication, low cost, wide impedance bandwidth and transmitting and receiving wideband signals without significant distortions [79, 80].

4.1 Coaxial Fed Rectangular Patch Antenna for WLAN Applications

Microstrip antennas are also known as patch antennas. Due to their simplicity and ease of integration with circuit board technology, they become very popular antennas in the microwave frequency range [29]. The rectangular patch antenna is one of the most commonly used microstrip antennas. The simplest form of patch antennas is the pin-fed patch, which does not suffer from feed network radiation and simple to construct. This method is also known as probe feeding that is proposed and demonstrated in mid-1970 [81]. The outer conductor of the coaxial cable is connected to the ground plane, while the centre conductor is fed through a hole in the substrate and the ground plane and electrically connected to the patch element. The pin-feed also allows simple impedance control [82]. The feed-point is positioned so as to control impedance. The feeding pin is usually an extension of the centre conductor of a coaxial cable used to feed the

antenna. Figure 4.1 shows a cross-section for a rectangular patch antenna with the pin feeding.

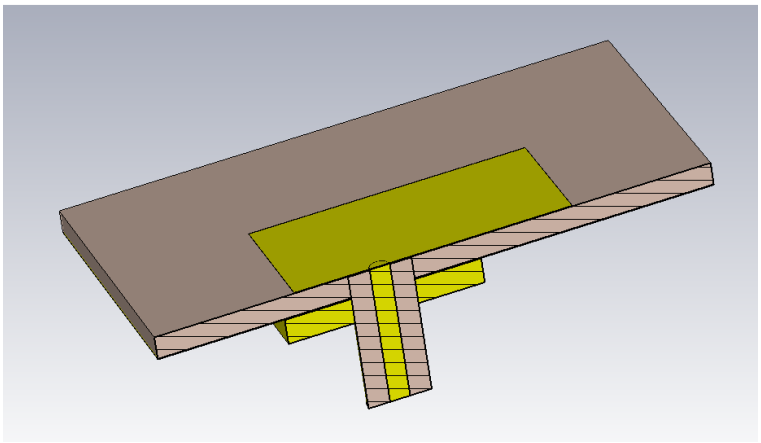


Figure 4.1. Cross section of a pin-fed rectangle patch antenna.

In general, the patch length controls the resonant frequency and the patch width controls the bandwidth and the impedance level. The larger the patch width, the smaller the input impedance of the antenna implemented on thin substrates usually less than $0.03\lambda_0$ [83]. The resonant length should be less than a half wavelength due to the fringing effect. In addition, the substrate material relative permittivity ε_r need to be taken into account. So the general equation for the rectangular patch length (L) is [28, 29]:

$$L = 0.49\frac{\lambda_0}{\sqrt{\varepsilon_r}} \tag{4.1}$$

Equation (4.1) is considered a good starting point for simulation. While equation (4.2) can be used taking in consideration the fringing effect of both patch antenna edges as following [30]:

$$L = 0.5\frac{\lambda}{\sqrt{\varepsilon_r}} - 2\triangle L \tag{4.2}$$

Where ΔL is the fringing length that can be calculated using equation (4.3) in which ε_{eff} is the effective substrate dielectric constant:

$$\triangle L = 0.412\frac{(\varepsilon_{eff} + 0.3)(\frac{W}{t} + 0.264)}{(\varepsilon_{eff} - 0.258)(\frac{W}{t} + 0.8)}t \tag{4.3}$$

The patch can be seen as a resonant cavity with radiating slots at each end of the patch. The fringing fields act to extend the effective length of the patch, with the result that the length of the half-wave patch is usually less than a half wavelength in the dielectric medium [26]. To increase the resonant frequency, the patch length should be decreased.

The patch antenna element is usually manufactured by etching it in a metallised substrate, or by bonding metal cut-outs to a bare substrate. Pin-fed patches are sometimes constructed without a substrate by suspending the patch over a ground plane using the feeding pin or by using additional isolated supports. Stand-alone antennas are often constructed with a coaxial feed connector in the ground plane [84].

Pin-fed patch antennas usually operate near resonance to obtain real-valued input impedance. The input impedance is determined by the position where the feeding pin is connected to the patch and can be used to control the real part of

the input impedance quite accurately. However, the inductance caused by the feeding pin can degrade the input match. The pin inductance increases as the substrate thickness increase and can prevent the input impedance from becoming real when thick substrates are used. Since thicker substrates are needed for patch antennas with higher bandwidths, the pin-fed patch antenna is unsuitable when higher bandwidth is required [85]. For approximately find the pin feeding point position from the edge of a half wave rectangular patch antenna (Δx_p), the input resistance for the patch antenna (Z_a) need to be calculated, noting that the reactance is zero at resonant and the required matching impedance $Za(\Delta x_p)$ is 50 Ω [86]:

$$Z_a = 90\frac{\varepsilon_r^2}{\varepsilon_r - 1}(\frac{L}{W})^2 \tag{4.4}$$

and

$$Z_a(\triangle x_p) = Z_a \cos^2 \frac{\pi \triangle x_p}{L} \tag{4.5}$$

thus

$$\triangle x_p = \frac{L}{\pi}\cos^{-1}\sqrt{\frac{Z_a(\triangle x_p)}{Z_a}} \tag{4.6}$$

A rectangular patch antenna for WLAN applications is designed on a 1.52 mm thick Rogers RO5880 substrate with a relative permittivity of 2.2 and a coper thickness of 35 µm. The centre resonant frequency selected to be 5.25 GHz. According to equations (4.1), the patch length and width is calculated to be 18.9 mm. The patch impedance at the edge found to be 363 Ω by using equation (4.4).

So the ping feeding point position found to be 7.16 mm by using equation (4.6). The initial return loss is shown in Figure 4.2. The length and pin position optimised to get better return loss for the patch at 5.25 GHz that is shown in Figure 4.3.

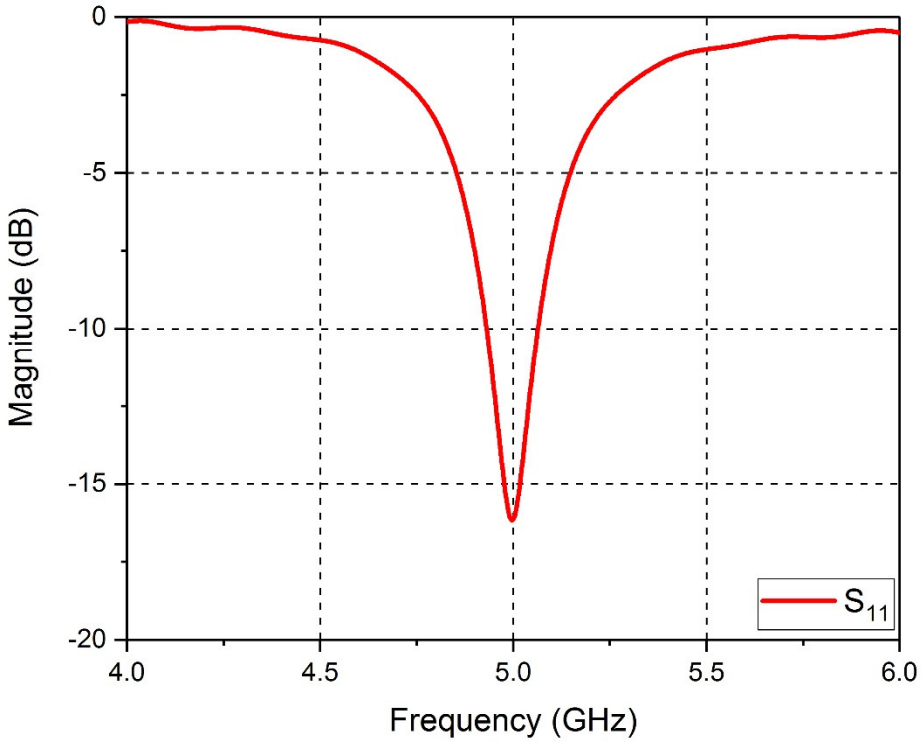


Figure 4.2. The S_{11} of the rectangular patch antenna before optimisation.

The patch antenna has a bandwidth of 160 MHz dB from 5.17 to 5.33 GHz. To increase the bandwidth, thicker substrates can be used or substrates with lower effective permittivity. The directivity also increases as the permittivity decrease because fabricating the patch antenna on a low permittivity substrate material produces an antenna with bigger physical dimensions. In addition, the directivity slightly increases as the thickness increases [83].

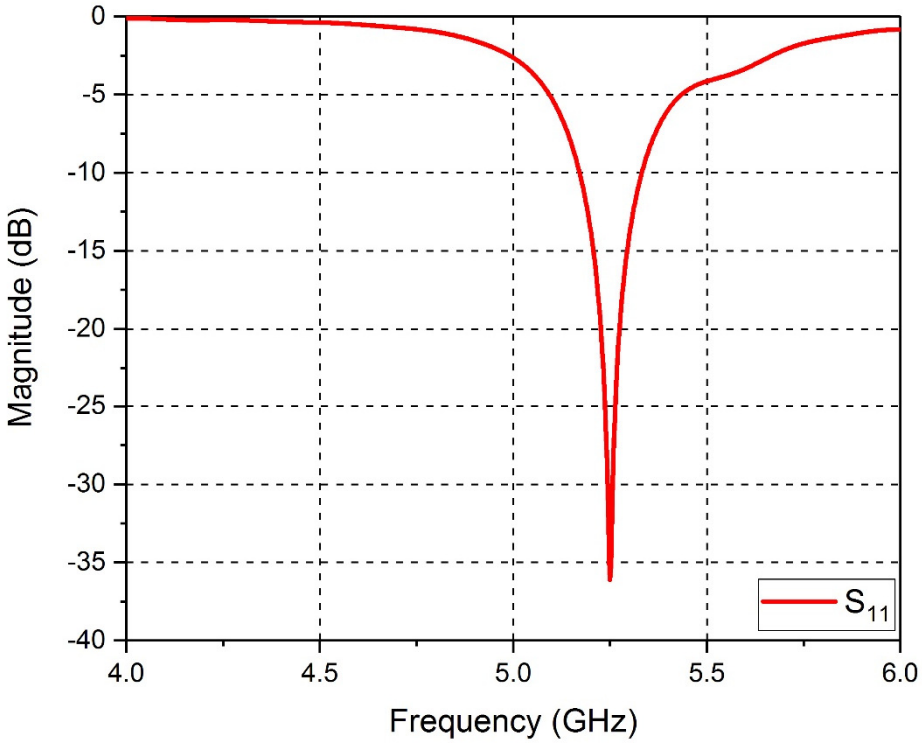


Figure 4.3. The S_{11} of the rectangular patch antenna after optimisation.

The pattern of a rectangular patch antenna is rather broad, with a maximum direction normal to the plane of the antenna and a null in directions tangential to the ground plane [26]. On smaller ground planes, the null-depth is reduced. On thicker substrates, the feeding pin may cause spurious cross polarised radiation [85].

The simulated radiation pattern for Φ =0 and 90° is shown in Figure 4.4 and Figure 4.5 respectively. As can be seen from these plots the radiation pattern is relatively broad in both orthogonal directions. The beamwidth is 83.6 and 80.1° when Φ = 0 and 90° respectively. The maximum gain is 7.11 dB with a main lobe direction of 0° and a side lobe level is -22.5 dB.

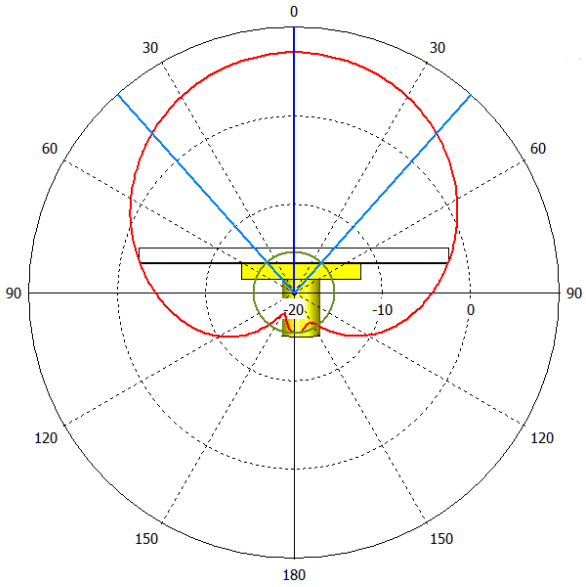


Figure 4.4. Rectangular patch antenna radiation pattern at 5.25 GHz for Φ=0°.

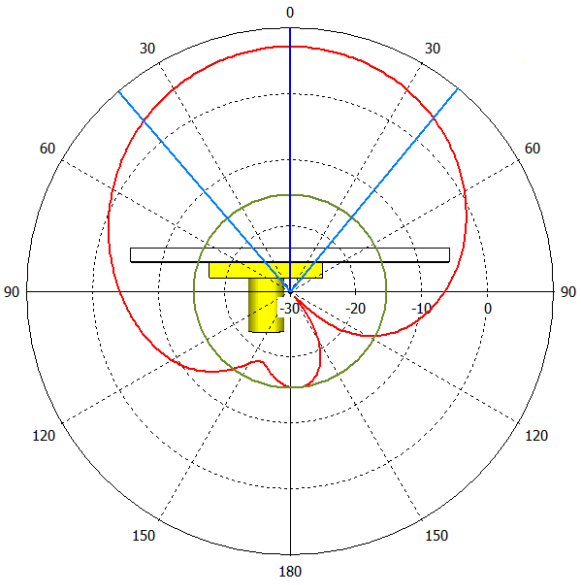


Figure 4.5. Rectangular patch antenna radiation pattern at 5.25 GHz for Φ=90°.

The fabricated antenna is shown in Figure 4.6, which shows the dimensions as well. The measured return loss is shown in Figure 4.7 that shows good agreement with simulation although the archived return loss is about 17 dB, which is less compared to simulation. That could be due to the parasitic capacitance and

soldering of the SMA connector. The measured radiation pattern is shown in Figure 4.8 and Figure 4.9 for both cutting planes Φ=0° and 90°, which reflects a good agreement between simulation and measurements.

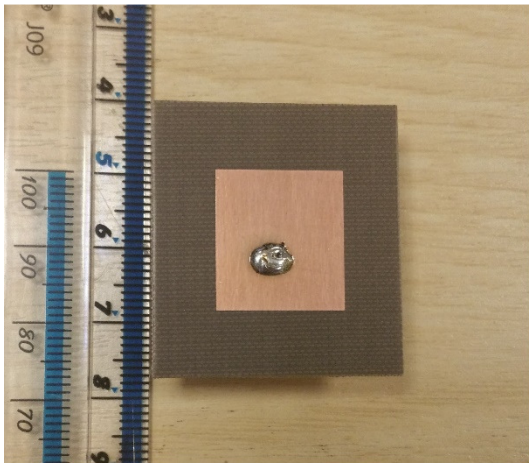


Figure 4.6. The fabricated rectangular patch antenna.

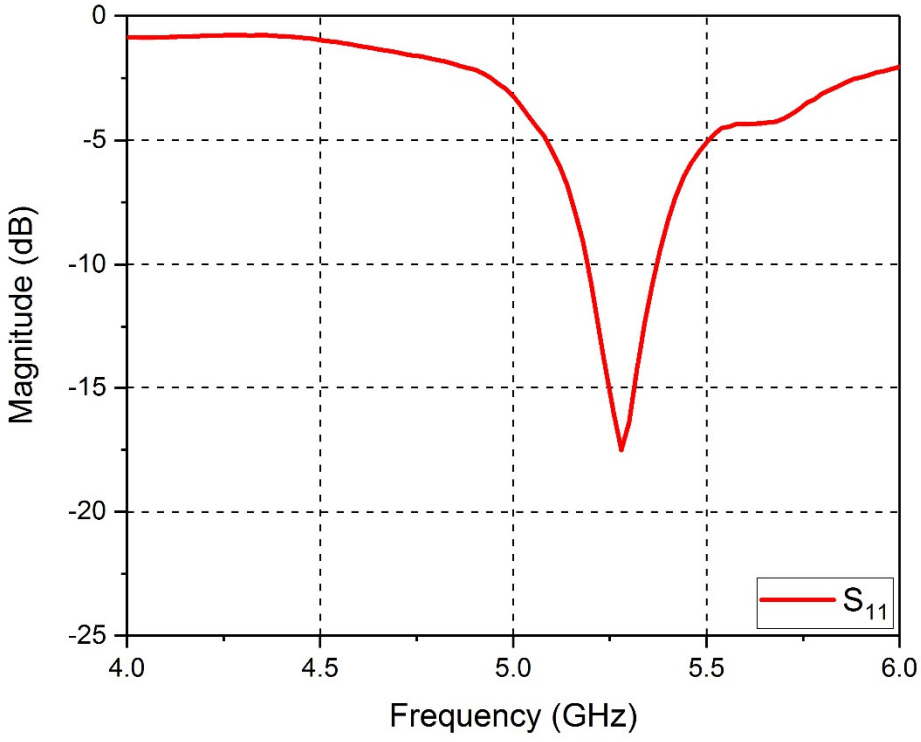


Figure 4.7. The measured S_{11} of the rectangular patch antenna.

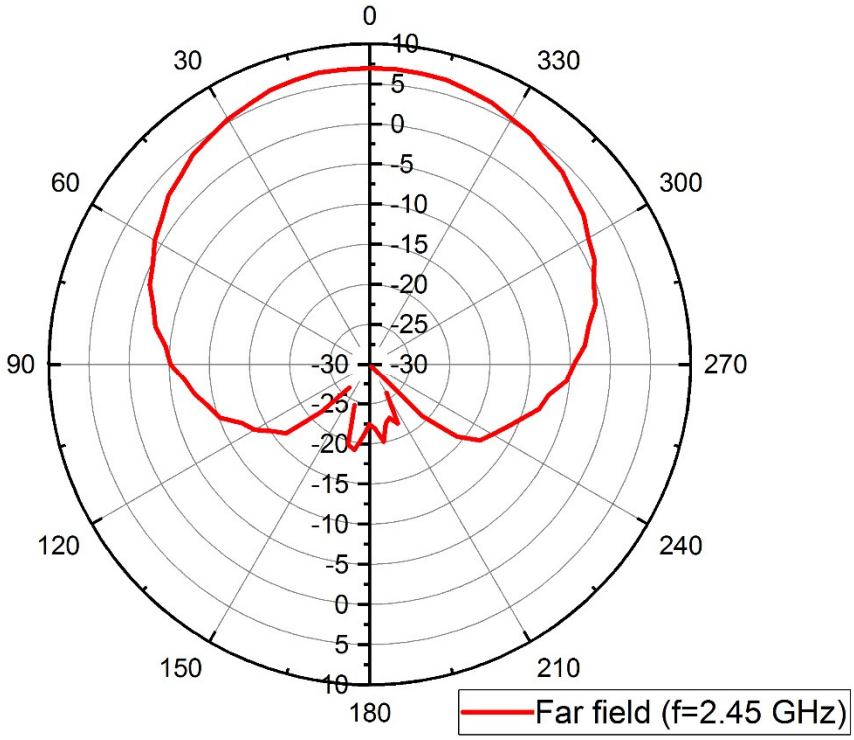


Figure 4.8. The measured rectangular patch antenna radiation pattern for Φ=0°.

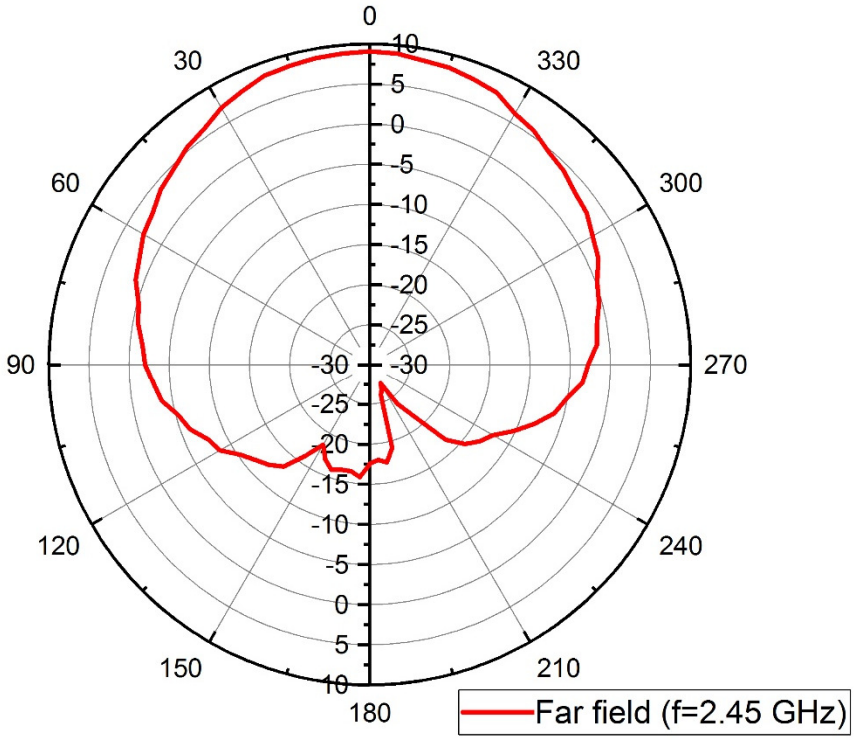


Figure 4.9. The measured rectangular patch antenna radiation pattern for Φ=90°.

4.2 Printed Microstrip-Fed Yagi-Uda Antenna for WLAN Applications

The Yagi-Uda antenna is a popular linearly-polarised, medium-gain end-fire array consists of a number of linear dipole elements, one of which is driven directly, while the rest have current induced by mutual coupling [26]. The wire version is a practical radiator 3 to 3000 MHz band and the printed version may be used well into the mm-wave band [87]. It is inexpensive, has a reasonable bandwidth, and can provide a high gain up to 17 dB or more if multiple arrays are used. It has a unidirectional beam with moderate side lobes. The Yagi-Uda array was invented by Uda in Japan in 1926 but the first English written work is published by his colleague Yagi [88].

In free space, the driven element is resonant at slightly less than λ/2, typically 0.45 to 0.49λ [26]. The parasitic elements in the direction of the radiation that called directors are slightly shorter than the feed element, which is about 0.4 to 0.45 of λ long. The gain can be increased by adding directors to the front of the driven element with spacing about λ/2. In the case of the microstrip-fed version of the antenna, the reflector element also acts as the ground plane for the feedline. The element spacing is usually not much more than approximately 0.3λ. The presence of a substrate influences the length and spacing of all the array elements.

Printed Yagi-Uda arrays can be optimised for a variety of requirements, such as gain, impedance or bandwidth. However, there is a trade-off between the performance characteristics, as an example, increasing bandwidth reduces the obtainable gain. For optimum designs, the director spacing and lengths are not

uniform [89]. Such designs were initially accomplished experimentally [90] but are now optimised using numerical techniques. The dielectric substrate effect on all the array elements' length and spacing should be taken into account.

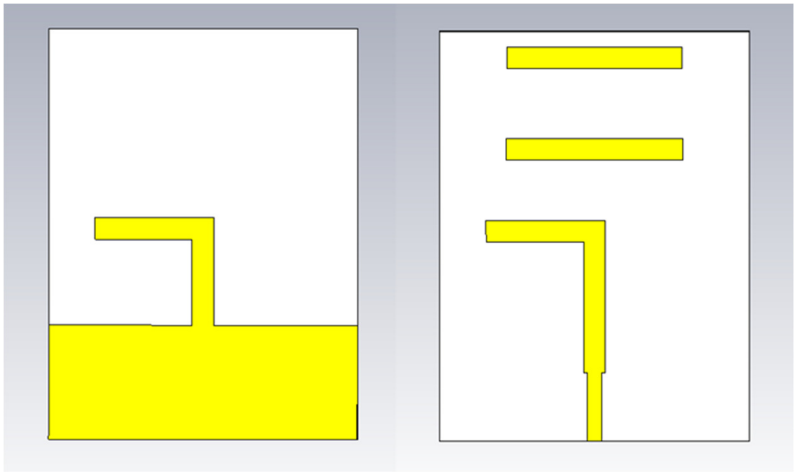


Figure 4.10. The designed microstrip-fed printed Yagi-Uda antenna.

A microstrip-fed printed Yagi-Uda array consists of a double-sided driven dipole element with a ground reflector and two of director elements, which is shown in Figure 4.10. This figure shows the four elements Yagi-Uda antenna including the reflector and the driven elements. The antenna designed to work in the 2.4 GHz frequency band and fabricated on an FR-4 substrate which permittivity is 4.3 and a thickness of 1.6 mm.

A balanced feeding is required to feed the driven elements. A double-sided printed dipole is used in order to realise the unbalanced microstrip feed line transition to the required balanced parallel strips line to feed the driven elements [87]. The non-driven or called parasitic elements have currents induced on them by mutual coupling as shown in Figure 4.11. Elements that are correctly spaced

have a similar current with a progressive phase shift, making the array essentially a structure supporting a travelling wave. The first element in this case also considered as a ground plane that is equivalent to a reflector and the elements beyond the driven element as directors.

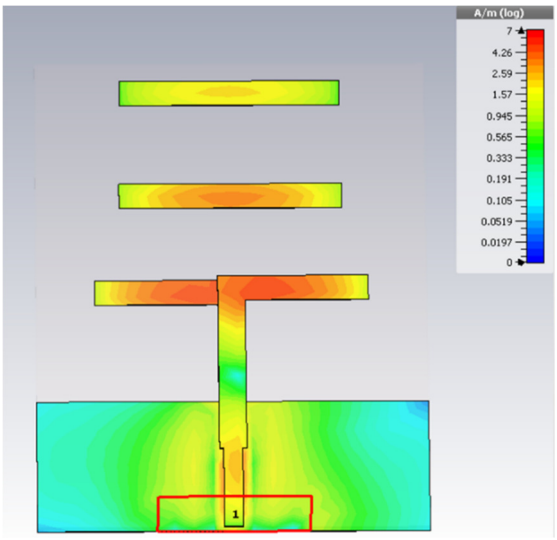


Figure 4.11. The current distribution of the designed Yagi-Uda antenna.

A Yagi-Uda antenna is typically optimised for different performance characteristics because it is difficult to describe typical performance. A high gain can be obtained but the impedance and bandwidth are relatively poor. For a conventional Yagi-Uda antenna, a wide bandwidth can be obtained, but this is at the expense of power gain [91].

The input impedance characteristic is extremely variable and a function of the element lengths and spacing. The dielectric constant of the substrate also lowers the input impedance. To increase the input impedance, the microstrip feed line width can be increased. Besides that, increasing the reflector spacing also

increases the impedance. However, changing the reflector spacing will also affect the back lobe and thus the front-to-back ratio.

Figure 4.12 shows the simulated return loss for the designed Yagi-Uda antenna that clearly shows that the antenna satisfies 2.4 GHz WLAN applications. The maximum simulated gain at 2.45 GHz is 7.8 dB while the side lobe level is -11.8 dB. Figure 4.13 shows the 3D far-field radiation pattern of the designed antenna. By increasing the number of director elements the gain can be increased [28]. Besides that, the existence of the substrate reduces the gain of the Yagi-Uda antenna and lowers the dielectric constant, the higher the achieved gain. The simulated beamwidth is 60.9° when Φ= 0° while it is 82.9° when Φ =90°.

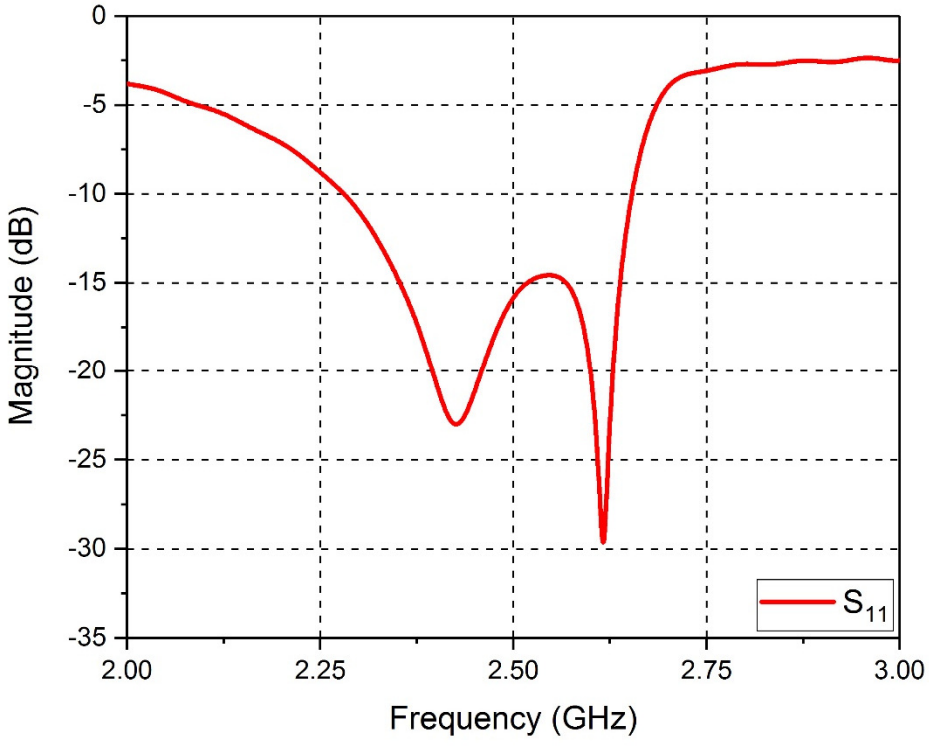


Figure 4.12. Simulated S_{11} of the Yagi-Uda antenna.

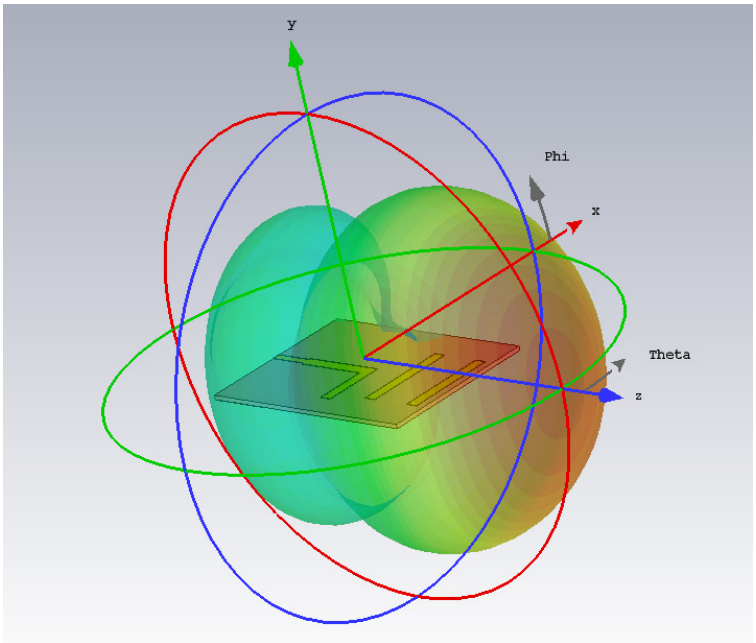


Figure 4.13. 3D far-field radiation pattern of the Yagi-Uda antenna.

The fabricated antenna is shown in Figure 4.14 and the design dimensions are listed in Table 4.1.

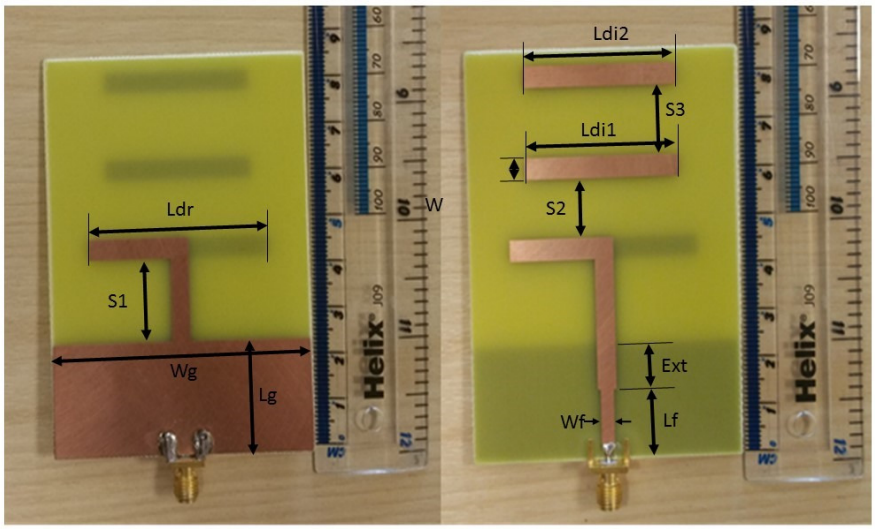


Figure 4.14. Photograph of the fabricated Yagi-Uda antenna.

Table 4.1. Designed Yagi-Uda antenna parameters.

Ldr	44.56 mm	W	4.46 mm
Lf	14.22 mm	Wf	3.09 mm
Lg	23.58 mm	Wg	63.67 mm
Ldi1	36.34 mm	LDi2	35.9 mm
S1	17.68 mm	S2	12.38 mm
S3	14.44 mm	Ext	9.36 mm

Figure 4.15 shows the measured return loss of the fabricated antenna. A good agreement can be observed by comparing it with Figure 4.12. Although, there is a slight frequency shifting that could be due to fabrication tolerance.

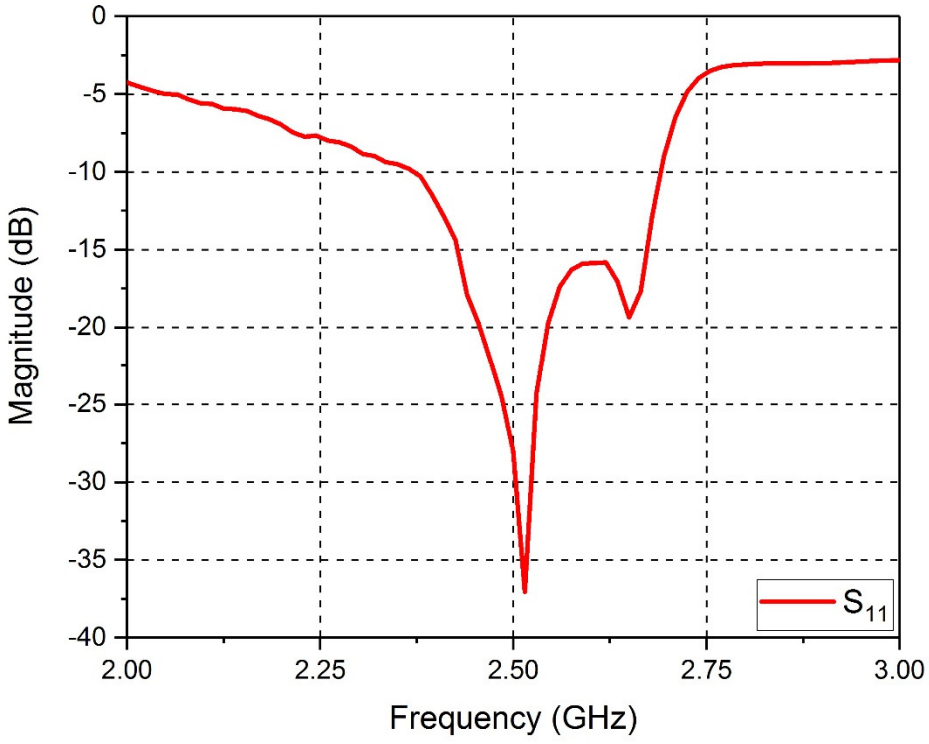


Figure 4.15. Measured S_{11} for the fabricated Yagi-Uda antenna.

The measured radiation pattern is shown in Figure 4.16 for Φ=0° cutting plane. The maximum measured gain is 7.2 dB compared to 7.8 dB simulated gain. The 3 dB beamwidth is about 58° compared to 60.9° in simulation and the main lobe direction is 0°. Figure 4.17 shows the radiation pattern for Φ=90° cutting plane. The maximum measured gain is 6.59 dB and the beamwidth is about 90° with a direction of 0°.

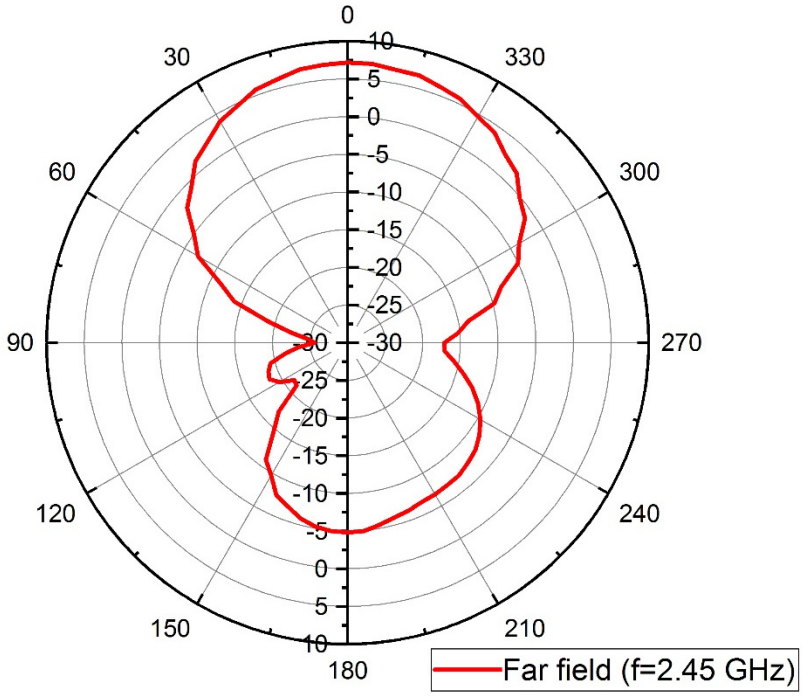


Figure 4.16. Measured radiation pattern for the fabricated Yagi-Uda antenna for Φ=0° cutting plane.

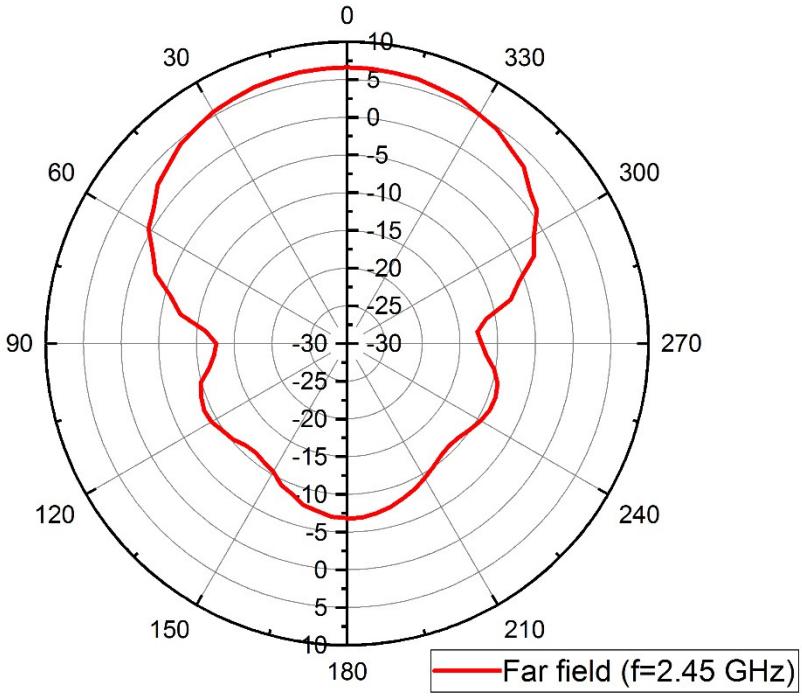


Figure 4.17. Measured radiation pattern for the fabricated Yagi-Uda antenna for Φ=90° cutting plane.

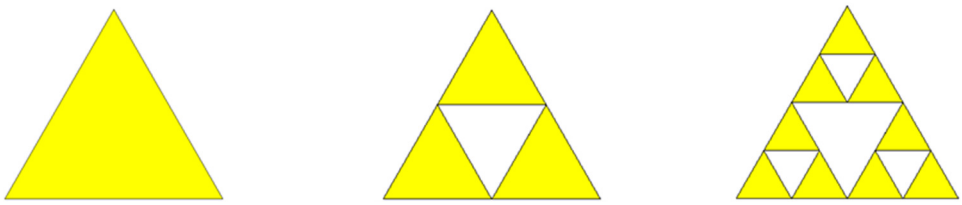
4.3 Microstrip-Fed Dual-Band Patch Antenna for WLAN Applications

This section is based on a published paper [92], a low-cost dual-band printed antenna that employs Sierpinski fractal geometry is presented in this section for the possible integration to IEEE 802.11n WLAN standards access points. The designed antenna covers two wireless spectrum bandwidth, they are the 2.4 and the 5 GHz bands. The antenna geometry is confined within a compact size of 75 mm x 75 mm x 1.52 mm. The antenna is mounted on a partial ground and fed by a microstrip line. It is modelled and optimised using CST Microwave studio and the results in terms of the reflection coefficient, VSWR, bandwidth and power gain are illustrated and compared to previously published literature. The antenna covers dual band with acceptable radiation performance. First resonance frequency centred at 2.45 GHz while the second at 5.5 GHz.

One of the important objectives in radio communication systems is the design of wideband, or even multiband, small antennas with a low profile for employment in commercial communications systems. The fractal antenna believed to be a useful technique to design small and multi-band antennas, and display space filling properties that can be exploited to miniaturize standard antenna elements, like as dipoles and patches [26, 93], and overcome some of the limitations of small antennas. Part of solutions of this limitation is that fractal antennas are compacted in small space.

The 802.11n standard offers several advantages over previous WLAN technologies. The most notable advantages are essentially improved reliability and greater application data throughput. The 802.11n standard acts in both the 2.4 GHz and 5 GHz bands, achieving the compatibility with pre-existing 802.l1a/b/g deployments. Wireless solutions depend on the 802.11n standard use various techniques to improve the reliability, throughput, and predictability of WLANs.

The antenna constructed using fractal geometry by scaling the initial triangle that is shown in Figure 4.18 (a) by one-half the generator. Application of the generator for the first time leaves three smaller filled triangles, the result is shown in Figure 4.18 (b), to which the scaled copy of the generator can be applied again. The corresponding structure is shown in Figure 4.18(c) [26, 93].



(a) (b) (c)

Figure 4.18. Fractal antenna geometry construction steps.

The configuration of the proposed antenna is shown in Figure 4.19. The second iteration of the Sierpinski geometry is considered. The antenna is fabricated on a 1.52 mm thick RO5880 substrate with a dielectric constant of 2.2 and a dimension of 75 mm × 75 mm. A microstrip line is used to feed the antenna with a dimension of 2 mm × 8 mm and has a partial ground with dimensions of 8 mm × 75 mm.

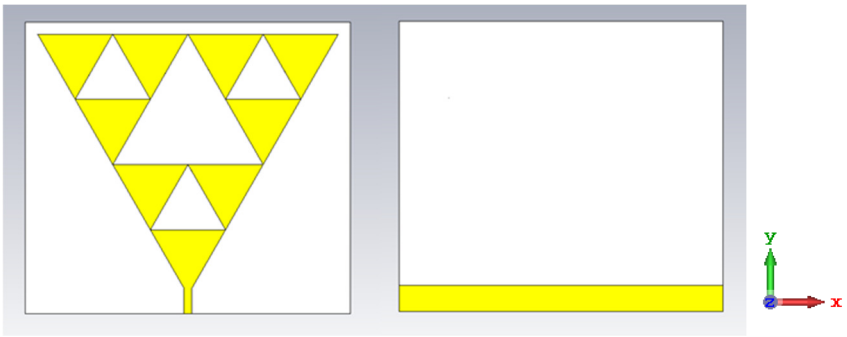


Figure 4.19. The feeding and ground layers of the designed Sierpinski antenna.

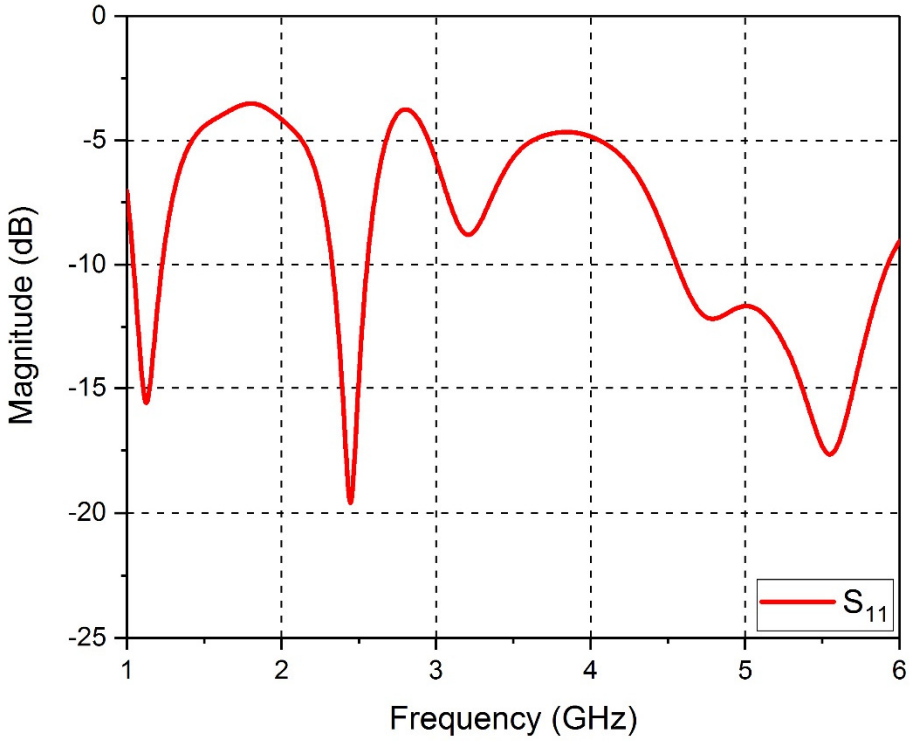


Figure 4.20. The S_{11} of the designed Sierpinski antenna.

The response of the return loss is shown in Figure 4.20. It can be noticed that the Sierpinski antenna is resonating at 2.45 GHz and 5.5 GHz with a return loss of 19.97 and 16.64 dB respectively. The antenna also exhibits two frequency bands that cover widely the two frequency spectrums for IEEE 802.11n standard. The 10 dB bandwidth is achieved at first resonant frequency centred at 2.45 GHz, which wraps all the fourteen channel of the 2.4 GHz band; in addition, the second bandwidth appears at a second resonant frequency centred at 5.5 GHz that in fact includes extensively the frequency range of 4.55 to 5.92 GHz.

Both operation frequencies are demonstrating wideband antenna characteristics is shown in Table 4.2. The input impedance of this antenna is found extremely sensitive to the width of the microstrip feed line. A parametric study is carried out

to find the optimum microstrip line width. Figure 4.21 shows the return loss plots for the antenna when the microstrip width changed from 1 to 4 mm with an increment of 1 mm in which an optimum value of 2 mm is found to satisfy both bandwidths requirements. The VSWR is an indication of how well the impedance of an antenna is matched, which describes the power reflected from the antenna. Figure 4.22 shows that the VSWR for the two operational frequencies is real and positive as shown in Table 4.2, where VSWR approaching one, that implies a matched load.

Table 4.2. Simulated Sierpinski antenna results.

f_0 (GHz)	Bandwidth for 10dB return loss		Return loss (dB)	VSWR
	(MHz)	%		
2.45	325	13.26	17.47	1.23
5.5	1310	23.8	11	1.26

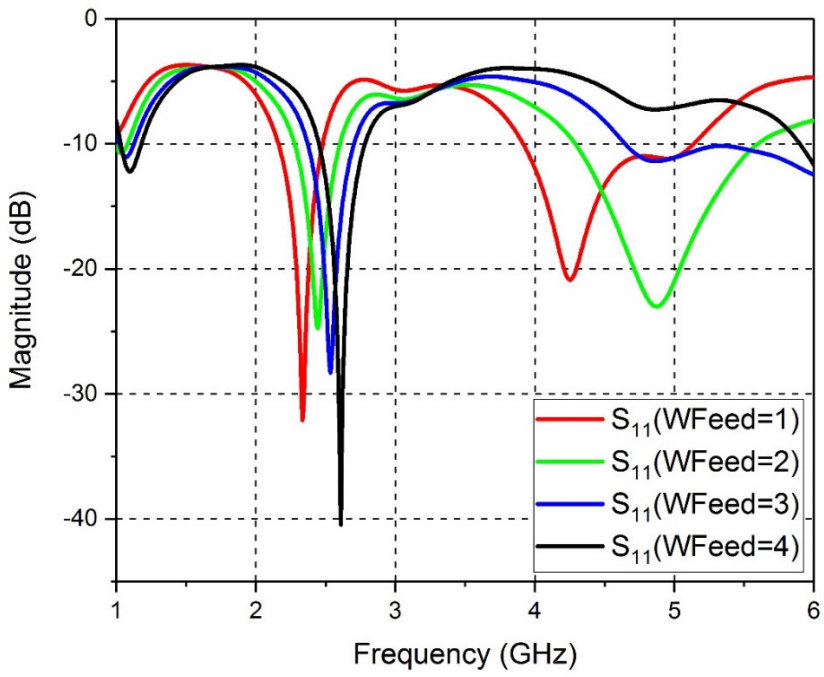


Figure 4.21. S_{11} for the Sierpinski antenna for different feed line width.

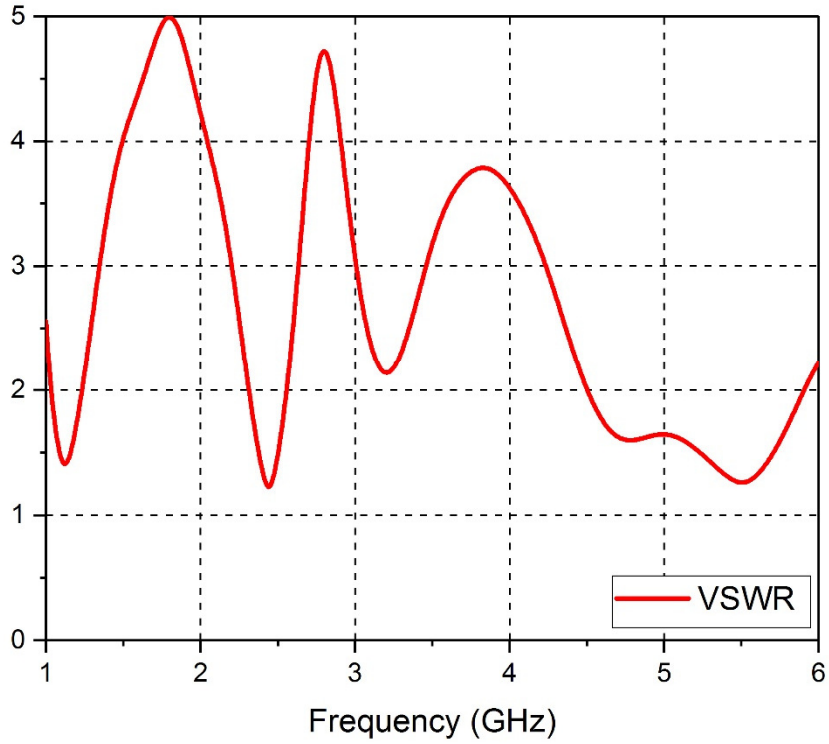
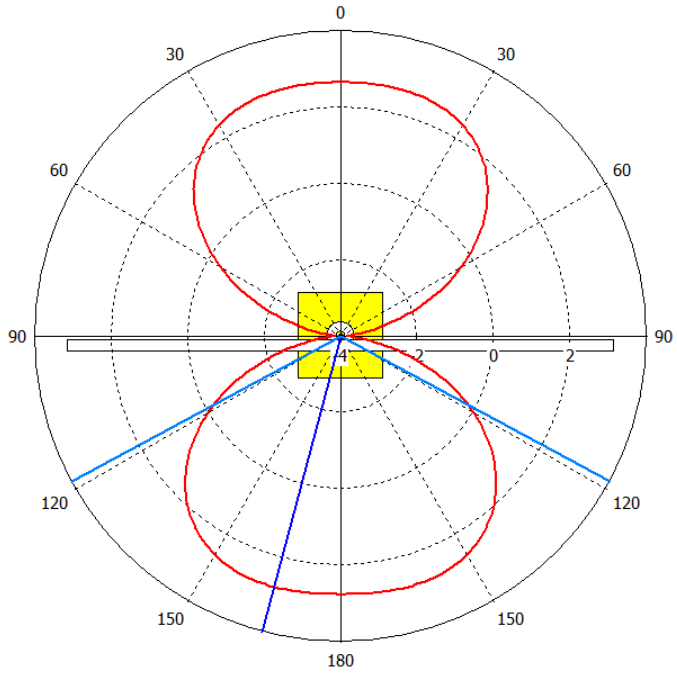


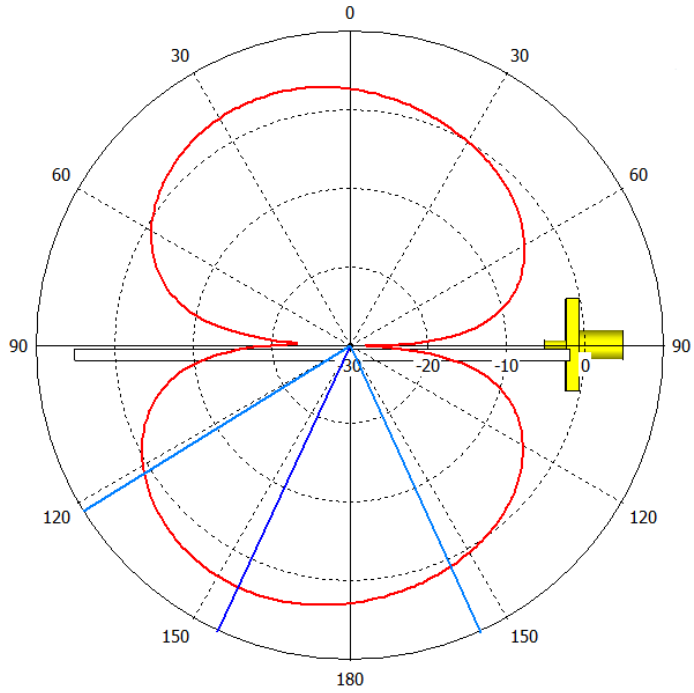
Figure 4.22. Voltage Standing Wave Ratio of the Sierpinski antenna.

The radiation patterns are shown in Figure 4.23 and Figure 4.24 for 2.45 GHz, and in Figure 4.25 and Figure 4.26 for 5.5 GHz, for cutting planes of Φ = 0 and 90° respectively. The radiation pattern is quite similar to the radiation from the monopole antenna, in which they showed an omnidirectional for both operational frequencies, apart from small variations appeared at higher spectrum band at 90° cut. The maximum simulated gain at 2.45 GHz is 2.78 dB and the beamwidth is 165° for the Φ=0° cutting plane. While the maximum gain is 3.83 dB and the beamwidth is 155° for Φ=90° cutting plane at the same frequency. On the other hand, the simulated maximum gain at 5.5 GHz is found to be 5.51 dB and the beamwidth is 55.8° for the Φ=0° plane whereas the maximum gain of 6.04 dB with a beamwidth of 42.6° is achieved at the Φ=90° cut plane.



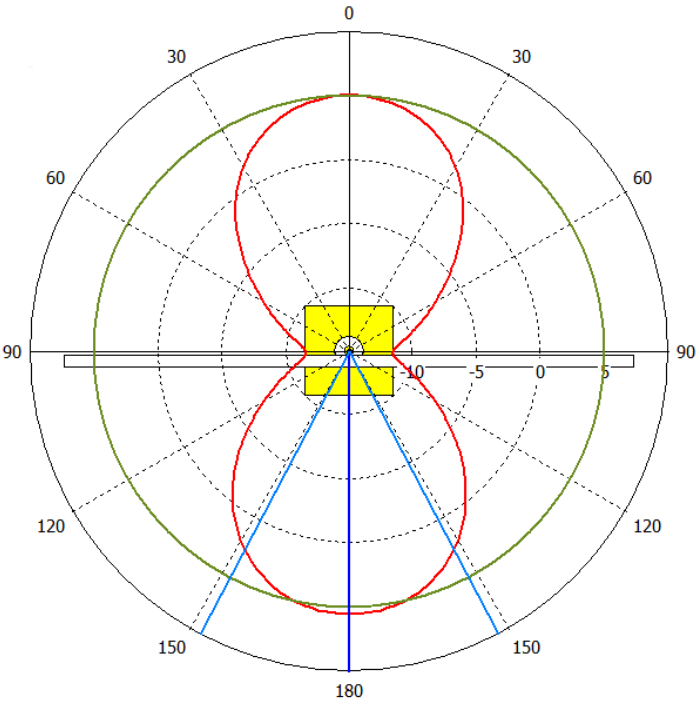
Frequency = 2.45 GHz
Main lobe magnitude = 2.78 dB
Main lobe direction = 165.0 deg.
Angular width (3 dB) = 123.2 deg.

Figure 4.23. Microstrip-Fed Dual band Patch Antenna simulated radiation pattern at 2.45 GHz for Φ =0° cutting plane.



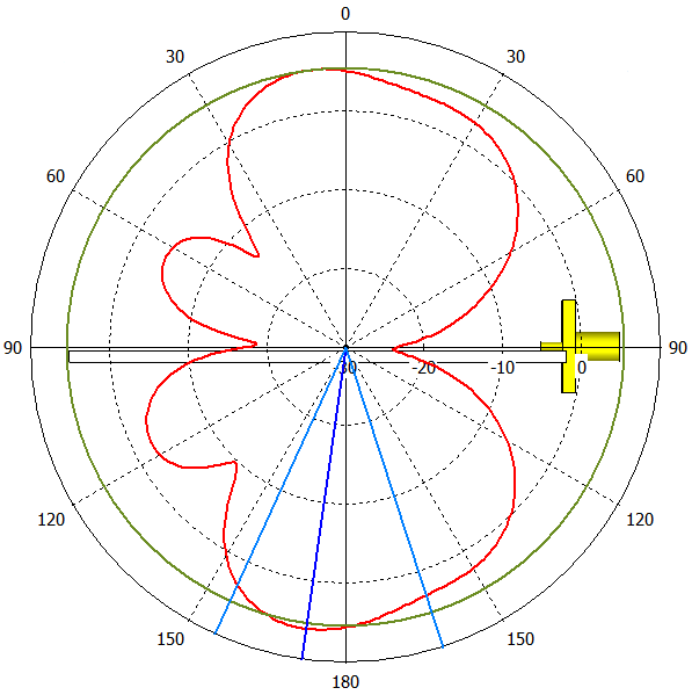
Frequency = 2.45 GHz
Main lobe magnitude = 3.83 dB
Main lobe direction = 155.0 deg.
Angular width (3 dB) = 82.8 deg.

Figure 4.24. Microstrip-Fed Dual band Patch Antenna simulated radiation pattern at 2.45 GHz for Φ =90° cutting plane.



Frequency = 5.5 GHz
Main lobe magnitude = 5.51 dB
Main lobe direction = 180.0 deg.
Angular width (3 dB) = 55.8 deg.
Side lobe level = -0.5 dB

Figure 4.25. Microstrip-Fed Dual band Patch Antenna simulated radiation pattern at 5.5 GHz for Φ =0 cutting plan.



Frequency = 5.5 GHz
Main lobe magnitude = 6.04 dB
Main lobe direction = 172.0 deg.
Angular width (3 dB) = 42.6 deg.
Side lobe level = -0.6 dB

Figure 4.26. Microstrip-Fed Dual band Patch Antenna simulated radiation pattern at 5.5 GHz for Φ =90 cutting plane.

A good agreement can be noticed by comparing the simulated return loss shown in Figure 4.21 when the microstrip width is 2 mm and the measurements result that is shown in Figure 4.27. The measured bandwidth for the lower frequency was 330 MHz that is extended from 2.27 to 2.6 GHz whereas for the upper frequency is around 1.23 GHz extended between 4.41 and 5.64 GHz. The measured radiation patterns for both operating frequencies for the two orthogonal planes are shown in Figure 4.28 to Figure 4.31. It can be seen that there is a good similarity between the measured and simulated radiation patterns. It is clear that the proposed antenna shows promising properties in terms of radiation performance, impedance matching, bandwidth and gain. One can deduce that the proposed antenna could be recommended as a possible candidate for IEEE 802.11n standards.

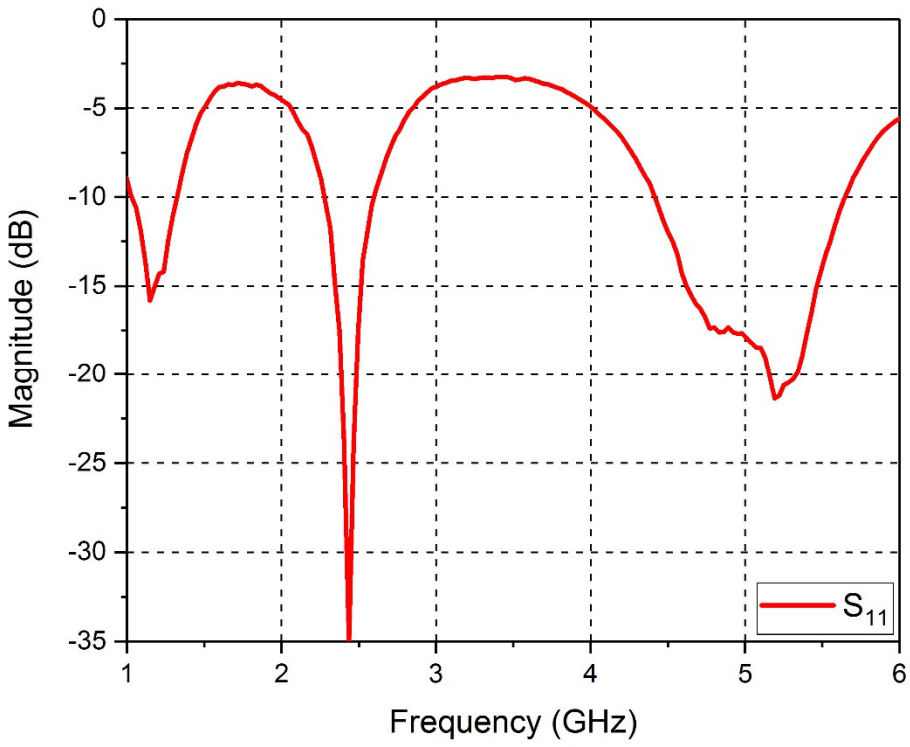


Figure 4.27. Microstrip-Fed Dual band Patch Antenna measured S_{11}.

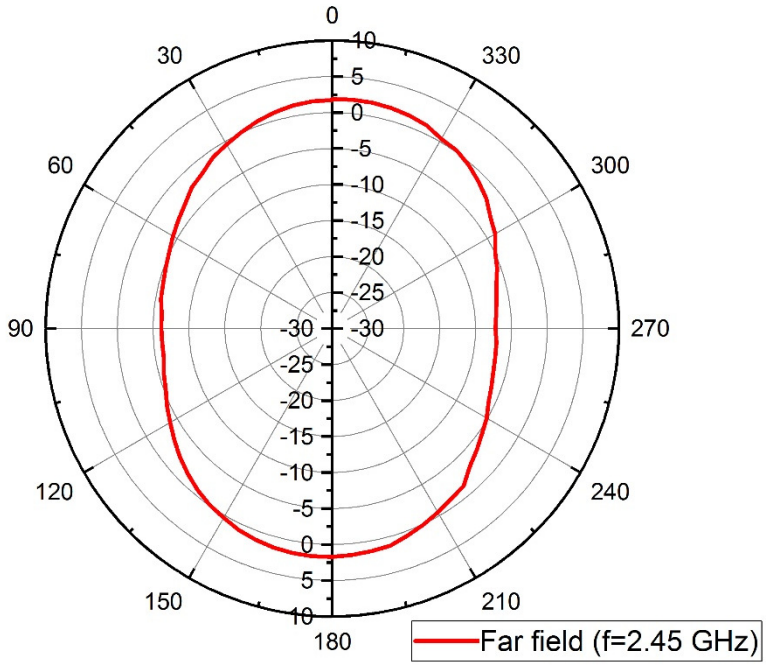


Figure 4.28. Microstrip-Fed Dual band Patch Antenna measured radiation pattern for Φ =0° cutting plane.

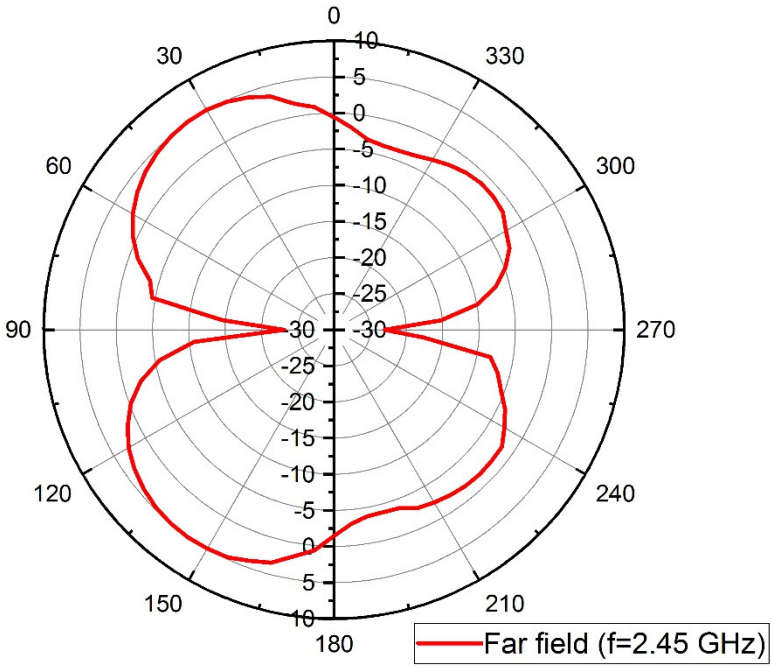


Figure 4.29. Microstrip-Fed Dual band Patch Antenna measured radiation pattern for Φ =90° cutting plane.

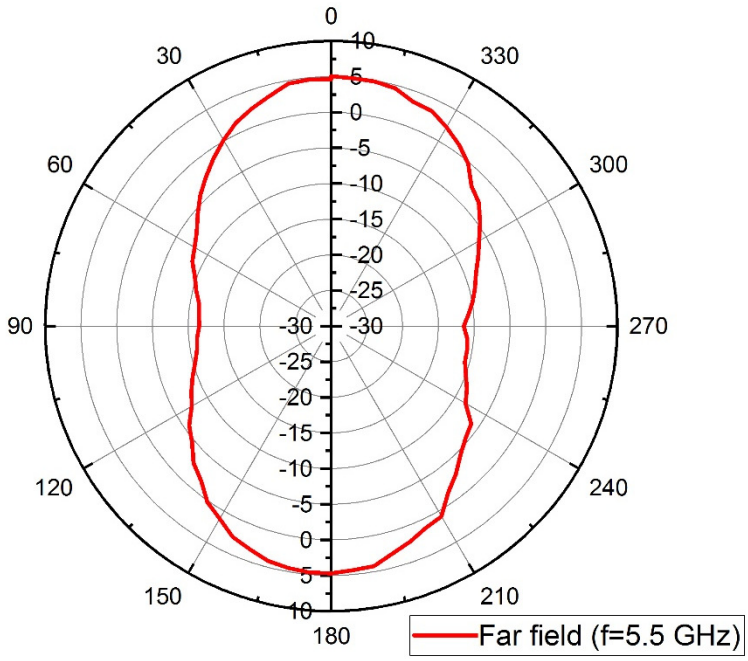


Figure 4.30. Microstrip-Fed Dual band Patch Antenna measured radiation pattern for Φ =0° cutting plane.

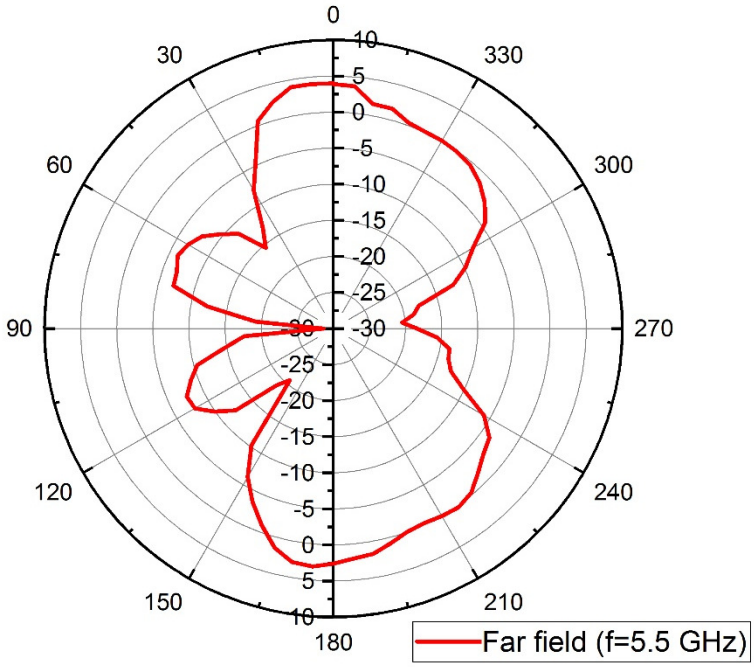


Figure 4.31. Microstrip-Fed Dual band Patch Antenna measured radiation pattern for Φ =90° cutting plane.

4.4 Summary

In this chapter, three different types of antennas were studied, designed, fabricated and tested to operate over single and dual bandwidths of the 2.4 and 5.2 GHz WLAN applications. The antennas were exhibited a good range of bandwidth covered and exceeded in some of them the standard range of the WLAN spectrum proposed by ITU regulations. The considered frequencies were covering the two well-known WLAN bands (2.4 and 5.2 GHz). The designed antennas exhibited minor different radiation performance but they preserved the Omni-directional feature for small antennas. The measured and simulated results showed a reasonable agreement in terms of the return loss, bandwidth and gain in which the resultant antennas could be recommended as a good candidate to be used for WLAN applications. The designed antennas in this chapter were embedded in chapter five in which antenna array configurations were applied with power dividers presented in chapter three.

Chapter 5

Antenna Array Applications

5.1 Embedded Power Divider Feeding Network Application

A 2x2 antenna array is constructed using four coaxial fed rectangular patch antennas that are designed and optimized in section 4.1. An embedded Wilkinson power divider is needed to feed the array elements. A power divider with four output ports is designed to feed the array elements. The feeding network is designed to deliver equal power and phase signal to the array. A four-port power divider constructed by using three 1 to 2 Wilkinson power dividers using similar technique presented in section 3.1.4. The feeding network placed below the array in a way that both the array and the feeding network shares a common ground that helps to reduce the radiation effect of the feeding network.

The impedance of the quarter wave transformer found to be 70.7 Ω using equation (2.26) and the SMD isolation resistor value found to be a 100 Ω using equation (2.27). The substrate used for this design is a Roger RO5880 with a thickness of 0.51 mm and a copper thickness of 35µm. Using equations (3.2) to (3.5) the initial design parameters are found then optimized to get better performance.

The fabricated single section equal power and phase power divider is shown in Figure 5.1. The measured S-parameter is shown in Figure 5.2. The return loss is found to be below 10 dB from 600 MHz to 6.84 GHz. The insertion loss is 3.15

dB at the centre frequency. Three of these power dividers were used to construct the 1 to 4 power divider as shown in Figure 5.3. The first stage input and output ports are extended to align the output ports of the second stage with the patch feeding points of the array.

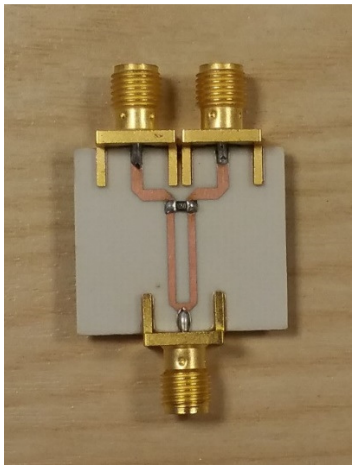


Figure 5.1. Fabricated equal power and phase Wilkinson power divider.

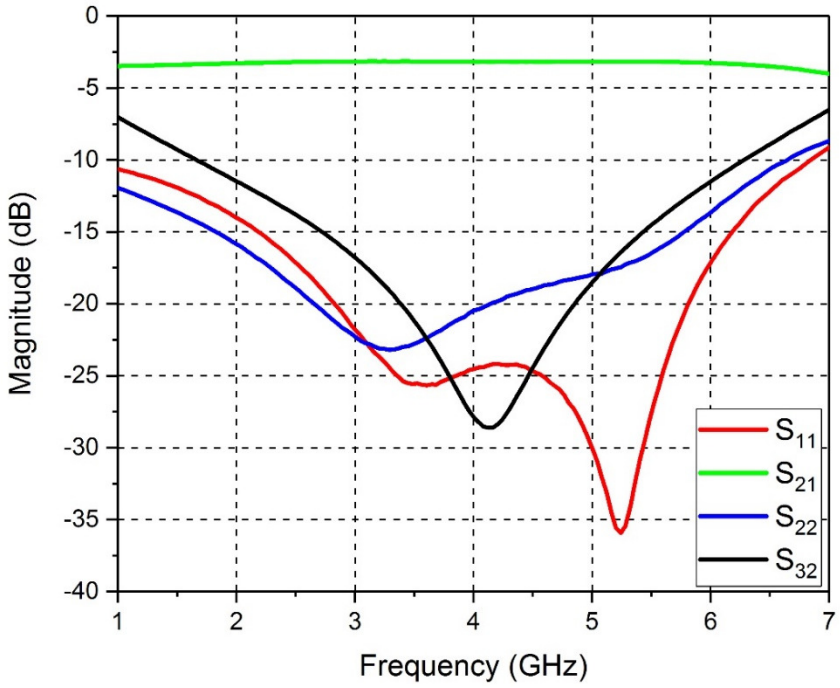


Figure 5.2. Measured S-parameter for the fabricated single section 1 to 2 Wilkinson power divider.

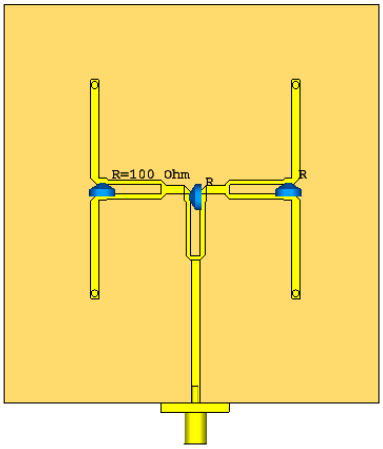


Figure 5.3. The designed power divider structure that is sharing a common ground with the patch antennas.

The horizontal and vertical spacing between the patches is optimized to be 21.28 mm. The simulated and measured return loss for the antenna array with the feeding network is shown in Figure 5.4.

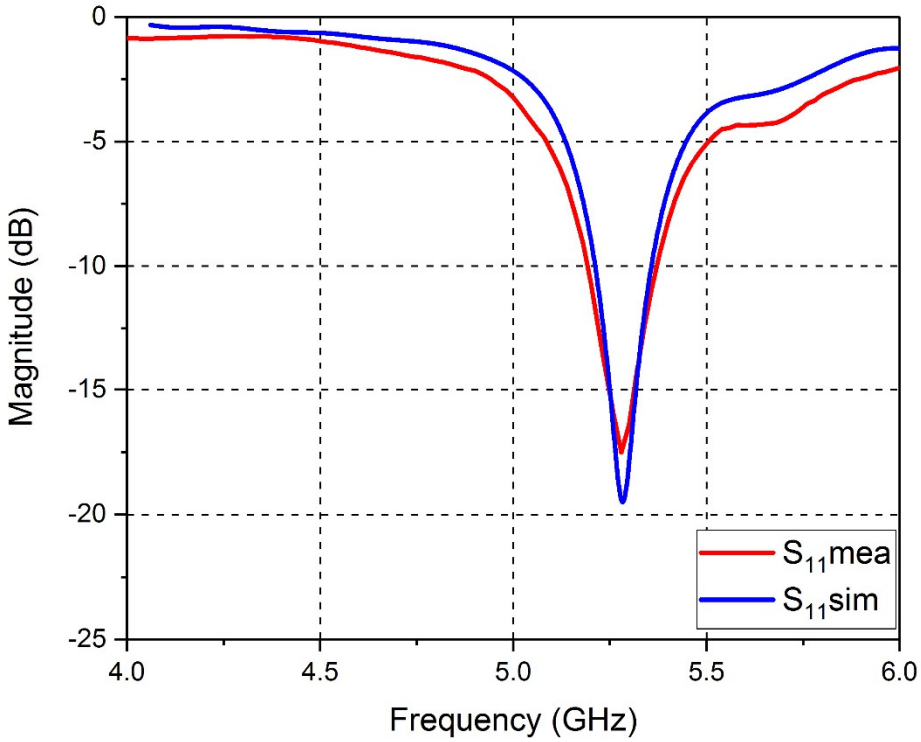


Figure 5.4. The simulated and measured S_{11} for the patch antenna array.

The measured bandwidth of the array is 180 MHz from 5.18 to 5.36 GHz. The array gain is 12.8 dB at 5.25 GHz as shown in Figure 5.5 that is 5.69 dB higher than the single antenna gain designed in section 4.1. The half power beamwidth is 40.2° and the main lobe direction is 0° for the cutting plane of Φ equals 0 as shown in Figure 5.5. The main lobe direction is 1° for the cutting plane of Φ equals 90° with a half power beamwidth of 36° as shown in Figure 5.6.

The fabricated array is constructed using Rogers RO5880 substrates which permittivity is 2.2. The array elements are fabricated on a 1.52 mm substrate, while the feeding network is fabricated on a 0.51 mm substrate. The antenna patches are fed using vias with a diameter of 1.3 mm. A good agreement is observed in Figure 5.4, Figure 5.5 and Figure 5.6 between the simulated and measured radiation patterns. The fabricated antenna array with the embedded feeding network is shown in Figure 5.7.

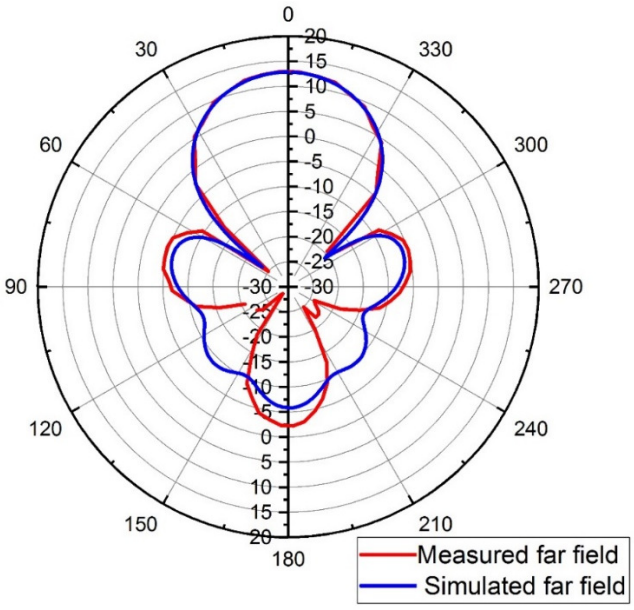


Figure 5.5. Simulated and measured rectangular patch antenna array gain at 5.25 GHz for Φ=0°.

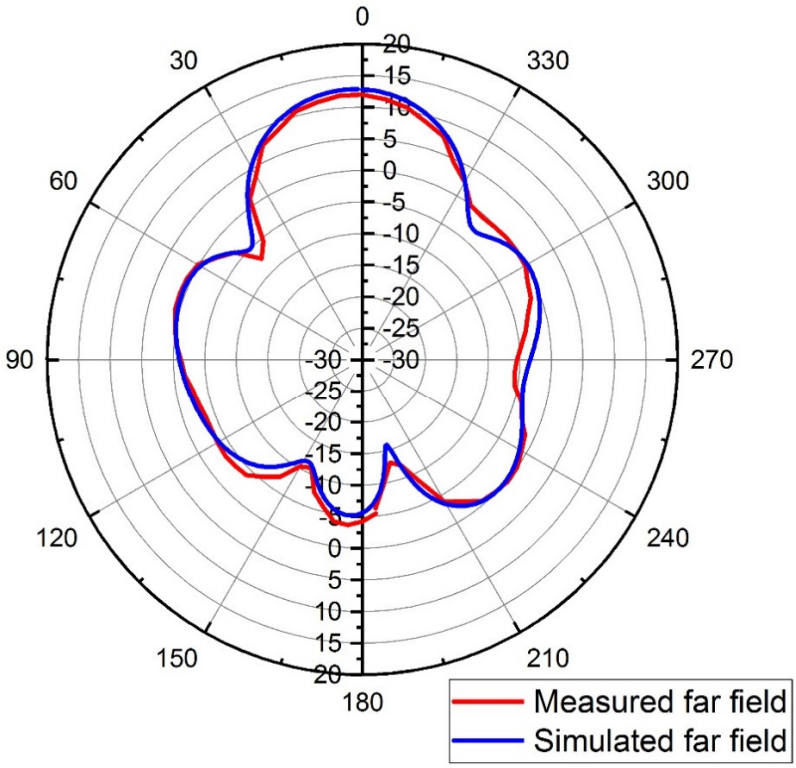


Figure 5.6. Simulated and measured rectangular patch antenna array gain at 5.25 GHz for Φ=90°.

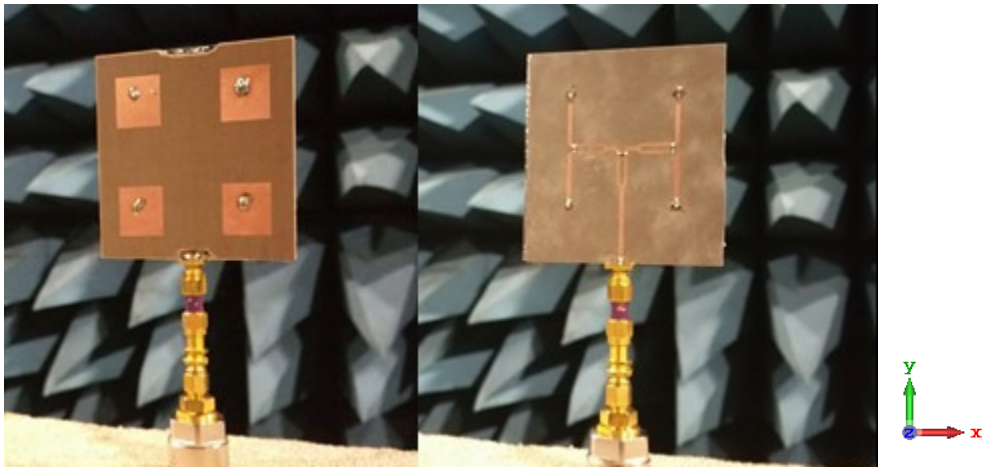


Figure 5.7. Fabricated patch antenna array in the testing anechoic chamber.

5.2 Multi-Layered Power Divider Feeding Network Application

An array of four Yagi–Uda antennas that are designed and optimized in section 4.2 is constructed benefitting from the multi-output ports power divider designed and optimized in section 3.2. The power divider provides an equal power and phase for each antenna element in the array and consists of three layers as discussed earlier. A cavity box is designed and fabricated in order to reduce the effect of the radiation of the power divider on the antenna array. The fabricated power divider with the cavity box is shown in Figure 5.8 while the cavity lid is taken off to show the power divider board. The output ports length is calculated so that the power divider dimensions with the cavity box and connectors fulfil the array spacing. The horizontal and vertical spacing is set to be 70 mm from the centre of each antenna element.

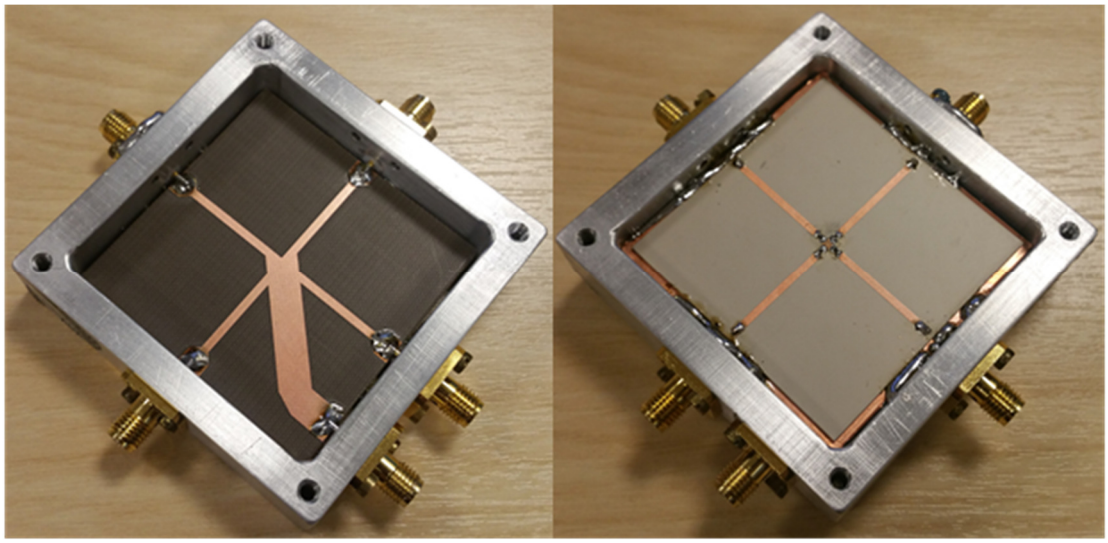


Figure 5.8. Multi-output ports power divider with cavity box.

The simulated and measured return loss for the array is shown in Figure 5.9. There is a good agreement between the simulation and measurement results.

The return loss is better than 10 dB for the band from 2.22 to 2.69 GHz that satisfies the 2.4 GHz WLAN applications.

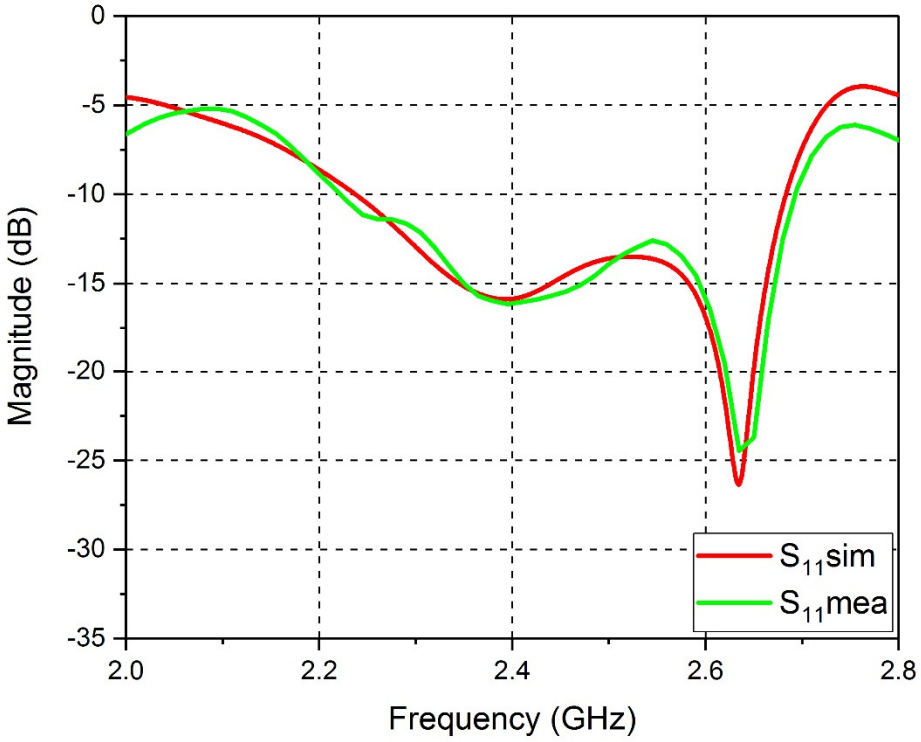


Figure 5.9. The simulated and measured S_{11} for the Yagi-Uda antenna array.

The cavity box is used to support the entire structure. Figure 5.10 shows the antenna array inside an anechoic chamber to measure the array radiation pattern. A flexible coaxial cable is used to feed the power divider to enable measuring the radiation pattern of the array for the required cutting planes.

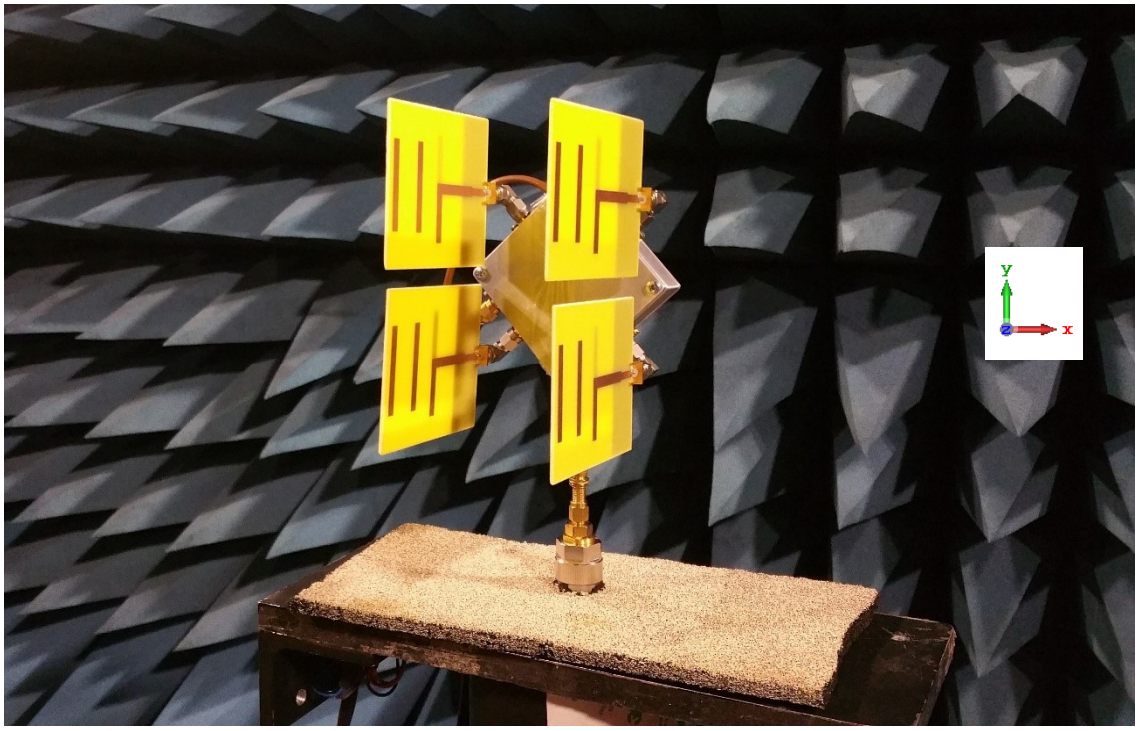


Figure 5.10. Yagi-Uda antenna array inside the anechoic chamber.

Figure 5.11 shows the simulated and measured radiation patterns for a vertical cutting plane of Φ=90°. It can be clearly seen that there is a quite good agreement between the results as expected. The achieved maximum measured gain is 11.2 dB compared to 12.3 dB simulated gain. The 3 dB bandwidth found to be 43.8° in which the main lobe direction is broadside pointed exactly at 0°.

Similarly, Figure 5.12 shows the radiation patterns for another vertical cutting plane at Φ =0°. Again, the simulated and the measured radiation patterns are shown a good agreement. The measured maximum gain found to be 11.52 dB compared to 12.3 dB simulated gain. The 3 dB bandwidth found to be 38.6° and the main lobe direction is 0°.

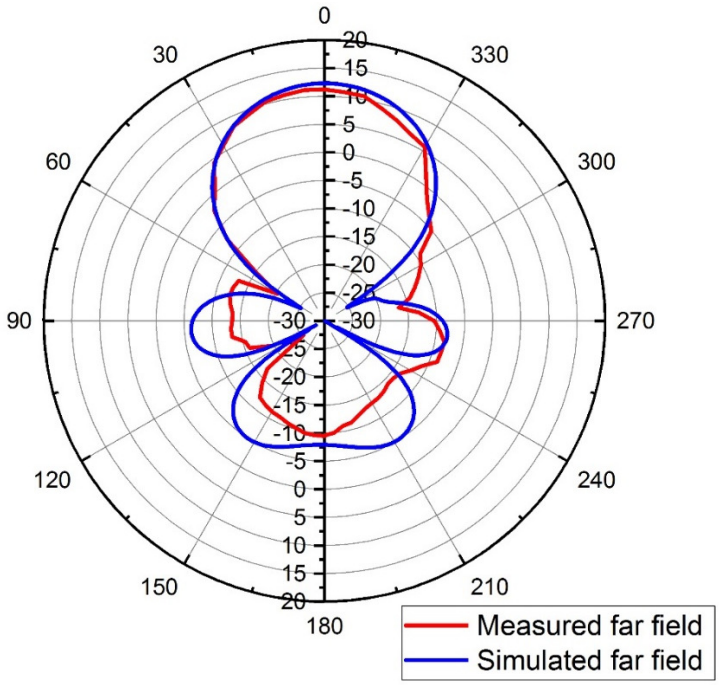


Figure 5.11. The simulated and measured radiation pattern of 2x2 Yagi-Uda antenna array when Φ =90°

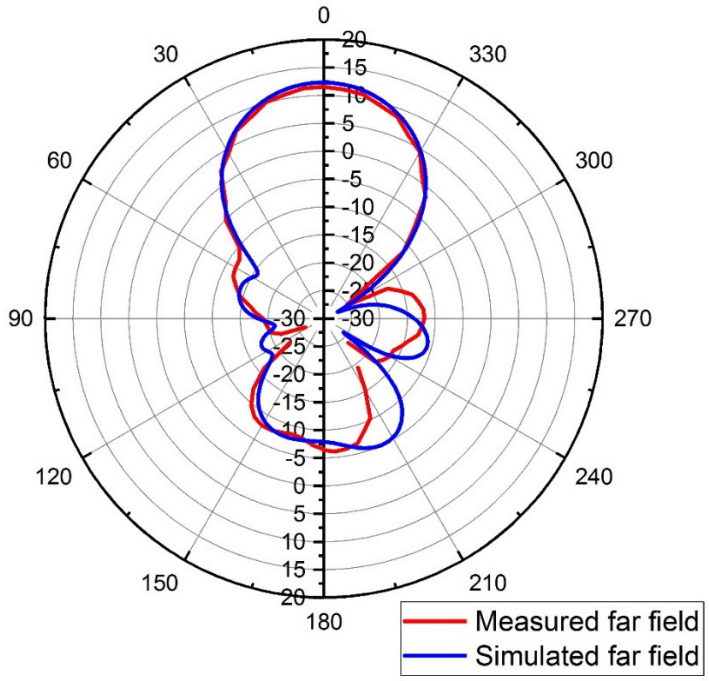


Figure 5.12. The simulated and measured radiation pattern of 2x2 Yagi-Uda antenna array when Φ =0°

5.3 Ultra-Wideband Power Divider Feeding Network Application

The radiation pattern of a single element antenna is wide and gives relatively low directivity and low gain. Although the radiation pattern of a single antenna may be designed with specific characteristics, in an array, the mutual coupling among the elements will affect the pattern of each element and they will act together to produce the total pattern. The performance of antenna array depends on a number of parameters such as the number of elements and the spacing between them, as well as the amplitude and phase of the excitation signals for each element [24, 94, 95].

Increasing the number of elements for a fixed spacing will lead to having a narrow beamwidth and increase the directivity, at the expense of increases the number of side lobes however the side lobes peaks decreases. Increases the spacing between the elements, which is usually represented by fractions of λ, leads to having larger grating lobes. A trade-off between the number of elements and spacing are considered in the design in order to compromise between side lobes level and the beam width.

An antenna array consisting of four dual-band antennas designed in section 4.2 is presented in this section. For the feeding network, the UWB equal split power divider that is designed in section 3.1 is used. The spacing between antenna elements is kept as small as possible to have wider beamwidth using four antenna elements. Figure 5.13 shows the antenna array with the feeding network inside the anechoic chamber.

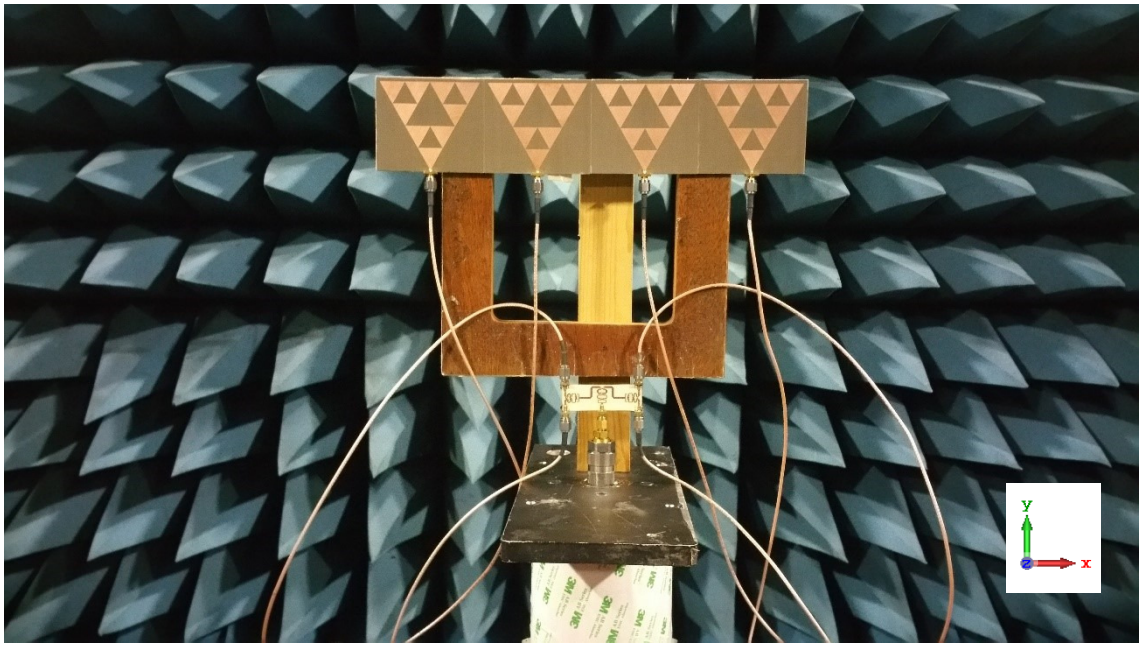


Figure 5.13. Dual-band antenna array with the feeding network.

The simulated and measured radiation pattern for the antenna at 2.45 GHz is shown in Figure 5.14 and Figure 5.15 for two vertical planes at Φ equals 0 and 90° respectively. The measured radiation patterns are well agreed with the simulated ones. The slight difference between the measurement and simulation could be due to the phase difference in the input signal for each antenna elements due to the use of the coaxial cable connecting the power divider output ports and antenna elements. The simulated and measured radiation patterns at 5.2 GHz are shown in Figure 5.16 and Figure 5.17 for both vertical planes at Φ equals 0 and 90° respectively. The difference between the achieved results was also deduced by the same reason above.

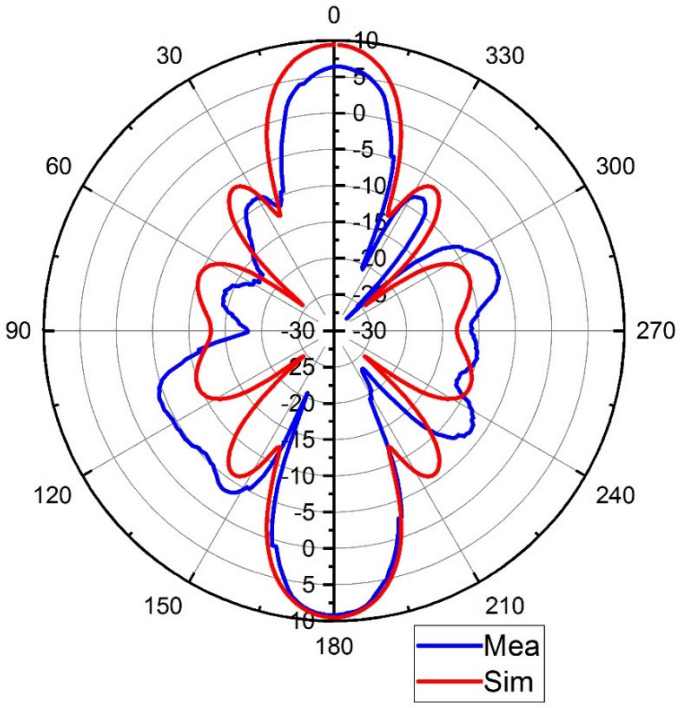


Figure 5.14. Dual-band antenna array radiation pattern for Φ=0° cutting plane at 2.45 GHz.

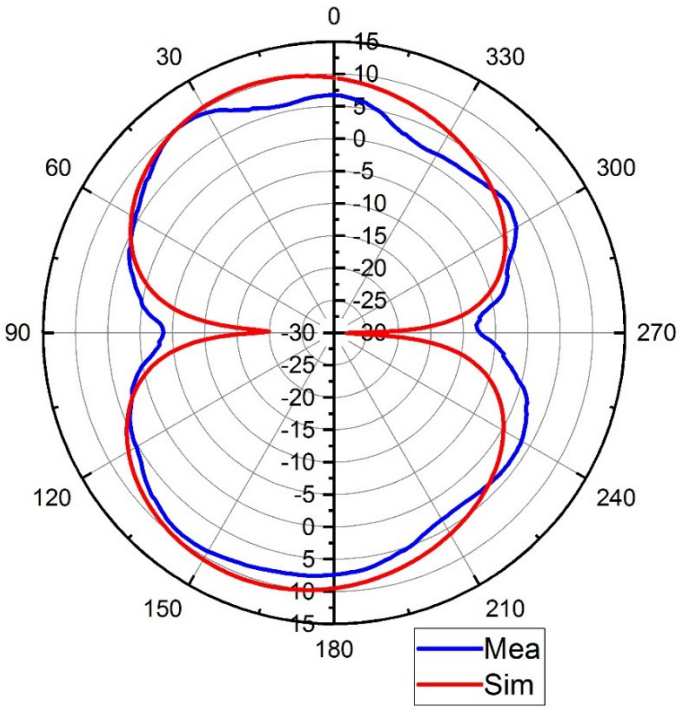


Figure 5.15. Dual-band antenna array radiation pattern for Φ=90° cutting plane at 2.45 GHz.

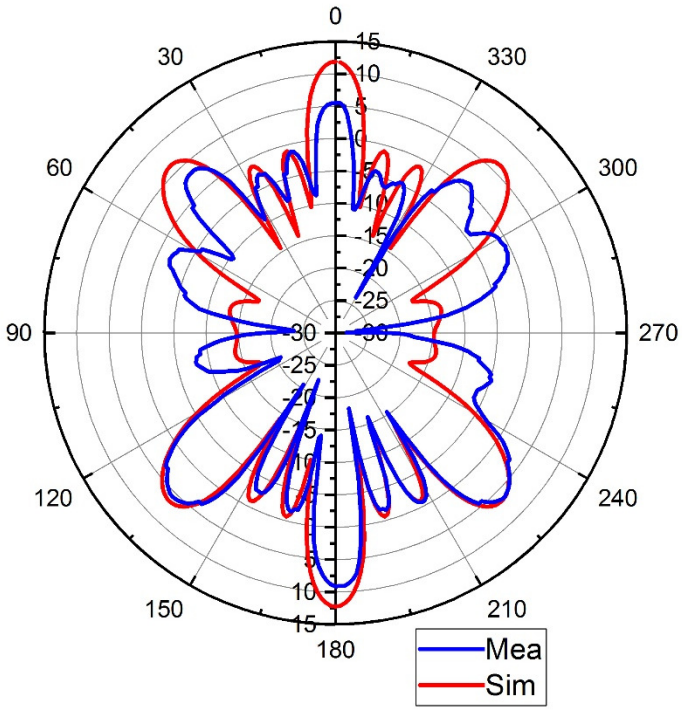


Figure 5.16. Dual-band antenna array radiation pattern for Φ=0° cutting plane at 5.2 GHz.

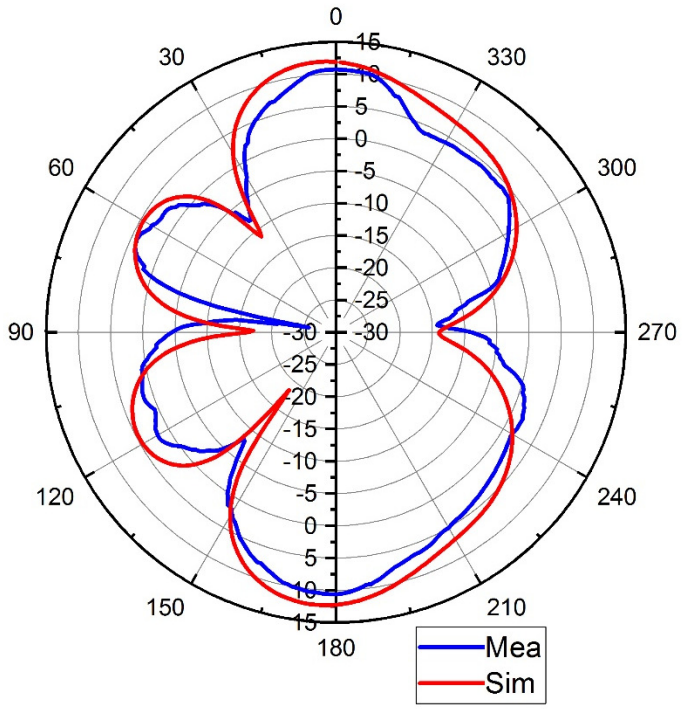


Figure 5.17. Dual-band antenna array radiation pattern for Φ=90° cutting plane at 5.2 GHz.

5.4 Reconfigurable Output Power Feeding Network Application

This section is based on a published paper [96]. The objective of this section is to present an application for the unequal division power divider with a practical application of self-interference cancellation technique for full duplex communication.

Recently, a considerable attention has been paid for full duplex communication as it allows transmitting and receiving information at the same frequency simultaneously in order to increase the spectral efficiency by two times by utilizing this type of communication. This section presents a new method of antenna cancellation with symmetric antenna placements to cancel the self-interference signal using an unequal power division power divider. Three monopoles antennas are modelled by using CST Microwave studio, one as a receiving antenna, while others as transmitting antennas. Moreover, many factors that could degrade the system performance are investigated. Results illustrate that this technique provides higher than 45 dB cancellation over a wideband frequency.

This section analyses the method of antenna cancellation with symmetrical antenna placements. In this technique, three monopole antennas are implemented, two as transmitting antennas, while the third as a receiving antenna. The monopoles diameter is 1.3 mm and the spacing between them is 66 mm. The unequal power divider that is designed in section 3.3 is used with extending one of its output ports by $\lambda/2$ at 5.2 GHz to supply the required 180° phase difference instead of a phase shifter to solve the problem of unequal amplitudes caused by the attenuation of the phase shifter [43]. The design

parameters are listed in Table 3.8. The new designed reconfigure power divider is shown in Figure 5.18.

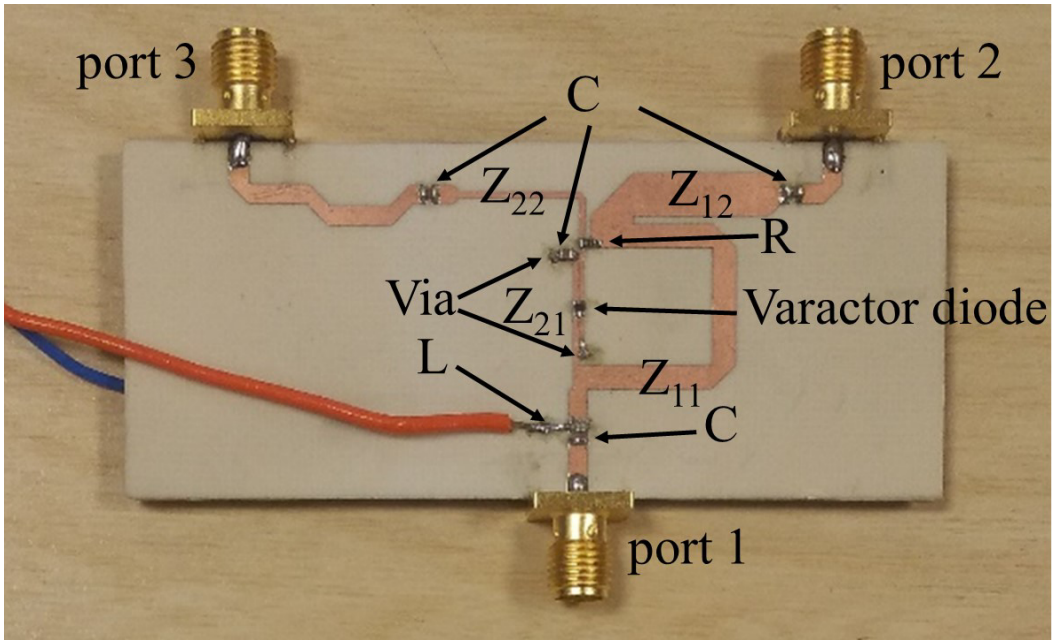


Figure 5.18. Reconfigurable power divider with 180° phase shift between output ports.

The two transmitters are placed at equal distances from the receiver. The receiver is located between the two transmitting antennas, and it is separated by 2λ from each transmitter. The two transmitters are fed by the outputs of the unequal power divider, which supplies a 180° phase difference and an equal power signal to the output ports. Consequently, the signals from the two transmitters will cross equal distances to reach the receiving antenna and cancel each other. The occupied space by this prototype is four and a half wavelengths that equal 26 cm at a frequency of 5.2 GHz.

This method provides higher cancellation over a wider frequency band. The reason behind that is that the unequal power divider can be reconfigured to provide two signals similar in amplitude with a 180° phase difference over a wide frequency band. Therefore, high self-interference cancellation over a wideband frequency can be obtained by using this technique. After the introduction of a second transmitting antenna, the total signal at the receiver is the sum of the (V_1) due to the first antenna and ($aV_1e^{-j\Phi}$) due to the second antenna, where (a) represents the signal attenuation and Φ is the phase shift provided by the power divider. The reduction factor RF can be defined as the ratio of the received power with one transmitting antenna and that with two receiving antennas:

$$RF = \left[V_1 / (V_1 + aV_1 e^{-j\phi}) \right]^2 \tag{5.1}$$

$$RF = 1 / \left[(1 + a\cos\phi)^2 + a^2 \sin^2 \phi \right] \tag{5.2}$$

This factor approaches infinity for the ideal case (a=1 and ϕ=180°), while the worst case value is 0.25 or -6 dB occurs when (a=1 and ϕ=0).

The reconfigurable power divider is fabricated on a Rogers RO4003C substrate and the monopole antennas fixed on a circular copper plate as shown in Figure 5.19. The reflection coefficient of the receiver antenna and the reflection coefficient of the two transmitters are shown in Figure 5.20. All return losses are better than 10 dB across the 5.2 GHz band. Additionally, the values of the isolation between the receiving and transmitting antennas can be considered

equal, the reason behind that is that the three antennas are almost identical, and the distance is similar between the two transmitters and the receiver. The values of isolation between the receiver and the transmitter antennas are approximately 20 dB at 5.2 GHz. These two values can be reduced by increasing the distance between the antennas, which leads to increase the cancellation performance. However, the size of the model will be larger.

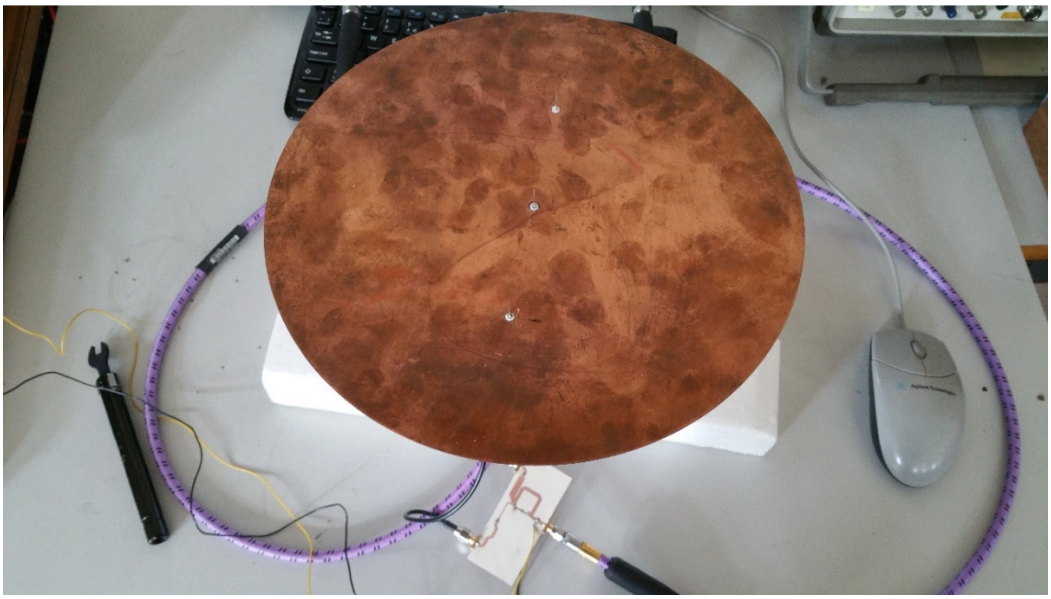


Figure 5.19. The fabricated self-interference cancellation system.

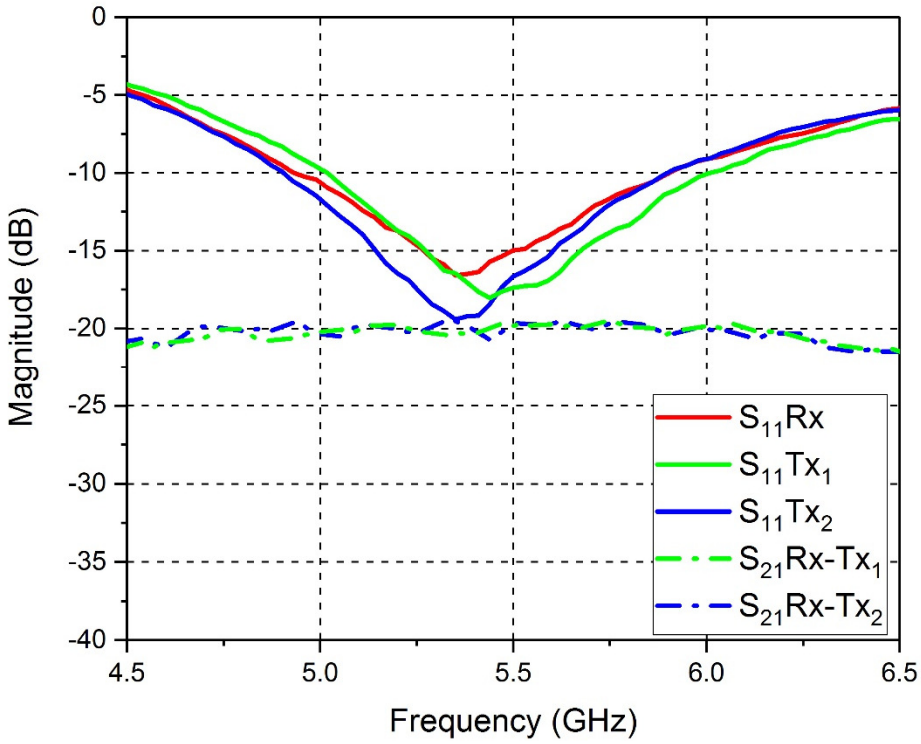


Figure 5.20. The monopols S-parameters.

Figure 5.21 illustrates the far field radiation pattern of the model at 5.2 GHz. It can be seen that two nulls in the far field region are produced, due to the 180° phase shift between the two transmitters. While using the two transmitting antennas can offer good cancellation by placing a null in the direction of the receiving antenna, the two transmitting antennas obviously have a radiation pattern that is different from that of a single one. There is a deep null in the direction normal to the axis of the three antennas. Therefore, the coverage of this arrangement is different from that of a single monopole antenna. The frequency response of the proposed method is limited by that of the feeding network and the used antennas.

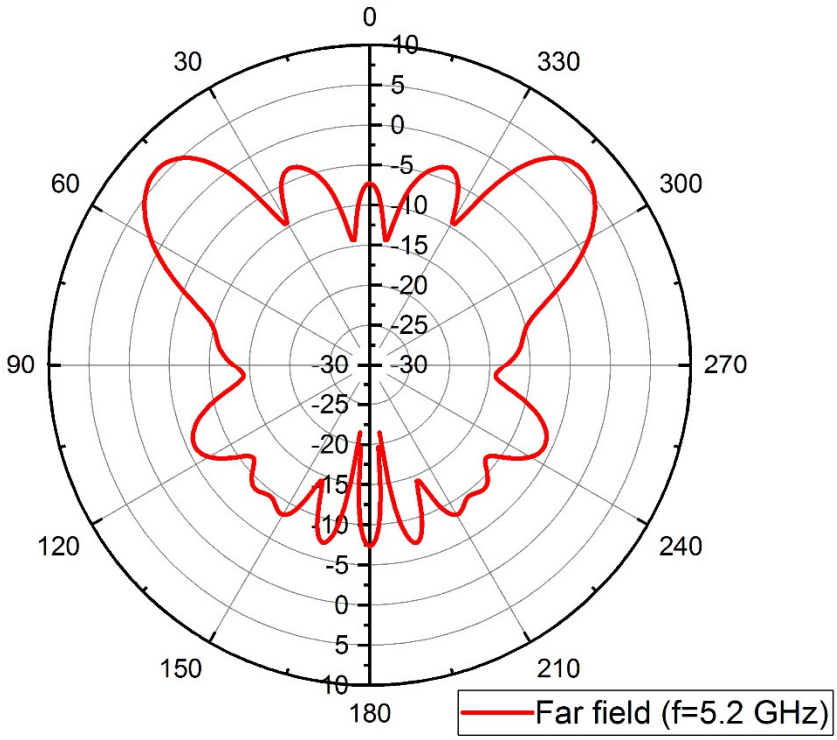


Figure 5.21. Transmitters radiation pattern at 5.2 GHz for Φ=0° cutting plane.

Figure 5.22 shows the cancellation performance over a wideband frequency, which is symbolized by S_{21}. It is clear that the value of S_{21} is below -45 dB across the range from 5.18 to 5.36 GHz and below -35 dB across the range from 5.09 to 5.46 GHz, while the minimum achieved S_{21} is 55.52 dB at 5.17 GHz.

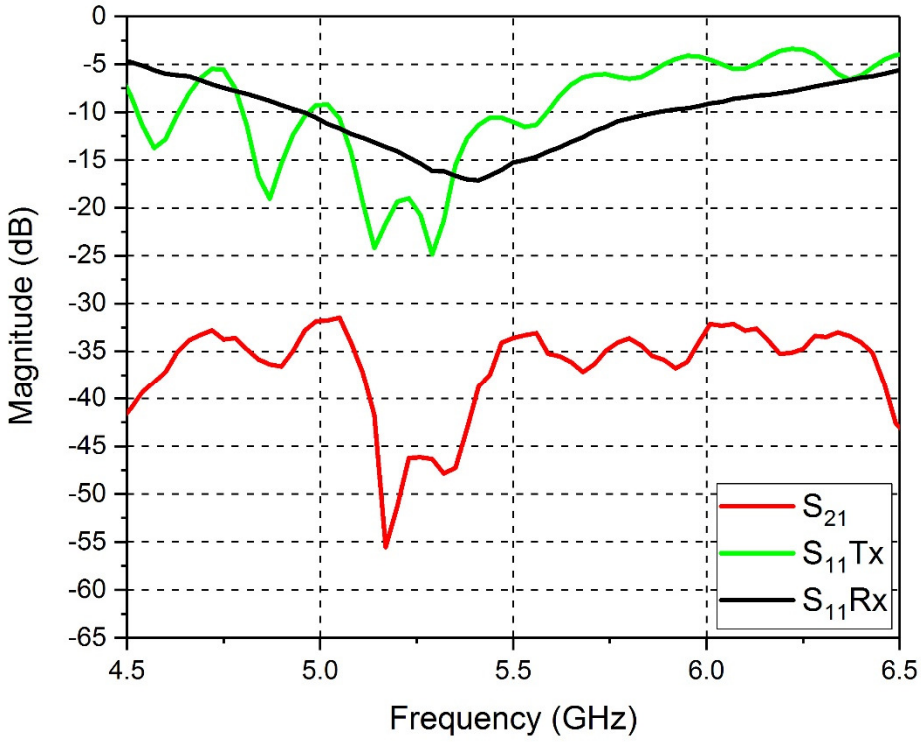


Figure 5.22. The measured S_{11} and self-cancellation performance.

5.5 Summary

Four array configurations were presented in this chapter. The array antennas approximate structural symmetry about the plane passing through the set's circuit board from the appropriate feeding network previously designed in chapter three. Each configuration proposed an application for the power dividers previously designed in chapter three that covered the 2.4 and 5.2 GHz WLAN bandwidths. The last section demonstrated the full duplex system of a two elements array supported by unequal power divider in which a self-cancellation better than 45 dB was achieved.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This work began by pointing out the different types of feeding networks related in principle to several antenna array applications. These types of feeding networks were presented over multiple and wide frequency spectrum bandwidths. The design of these networks were on uniplanar and multi-layered substrates having various material characteristics.

Several antenna array applications were presented in chapter five that provided promising array systems for WLAN applications. An important concept for adopting unequal power dividers for the full-duplex systems were presented in chapter five with a supporting practical example. That could establish a solid ground for implementing a full-duplex MIMO antenna system.

All aims and objective set out in chapter one for this work were achieved as shown below:

1. The design procedure of a miniature one to four UWB power divider was presented in section 3.1.4, in the form of a multi-section device, analysed and fabricated for UWB (3.1 to 10.6 GHz) applications. Close agreement between simulation and measurement results validated the design procedure. The fabricated power divider was compared with other works

and found to have better performance and to be smaller size. Furthermore, a miniature multi-output power divider was presented and used as a feed network for a UWB antenna array application as presented in section 5.3.

2. A novel five-way planar power divider was designed as an example of a general N-way planar Wilkinson power divider as shown in section 3.2. To overcome the isolation resistor crossover problem, when the number of output ports is greater than three, a third layer was introduced. To make the design and fabrication process easier, the microstrip feeding method was selected for the first time. The permittivity of the lower layer substrate was selected to be higher than the upper layer substrate, which made the quarter wave transformer physical length equal to the physical length of the half wavelength microstrip line interconnecting the isolation resistors. The proposed design reduced the need for cascading number of sections that reduced the conductor losses, thus enhanced the insertion loss. The practical measurements had good agreement with the simulation results that validated the design concept. For the wideband operation, very good isolation and insertion loss with very good amplitude balance that could propose the design as a good candidate for the industrial, scientific and medical radio band applications as shown in section 5.2.

3. A novel reconfigurable Wilkinson power divider was presented in section 3.3. The proposed power divider was capable to deliver equal and up to 8 dB output ports power difference. The power ratio was almost linearly proportional with the applied reverse biasing voltage on the varactor diode

ranging from 1 to 10.4 volt. A good amplitude stability was achieved between the output ports, which was below ± 0.1 and ± 0.2 dB for the unequal and equal output ports power difference scenarios respectively. The measured performance agreed with the simulation and proposed it as a good candidate for 2.4 GHz WLAN applications.

4. A simple full duplex system using symmetric antenna placement technique to cancel the self-interference signal was presented in section 5.4. The idea was based on placing two transmitting antennas at a similar distance far from the receiving one. The novel reconfigurable Wilkinson power divider that was presented in section 3.3 was used; however, one of the output ports was extended to provide a 180° phase shift between output ports. The model was designed to work on 2.45 GHz. The results showed that in perfect conditions, this technique provided more than 45 dB cancellation over a wider bandwidth.

6.2 Future Work

Market demands for miniature, compact and reconfigurable power dividers are growing so there is always a margin for improvement in feeding networks. This can be achieved by enhancing the performance of power dividers, reducing the size using proposed methods and achieving reconfigurability for higher frequencies and wider bands. The following points can be of interest for further research:

1. Power divider with a reconfigurable number of outputs can be designed. This can be archived by reconfiguring the impedance of the quarter wave transformers using a coupled line technique and a varactor diode similar to the technique presented in section 3.3. The coupled line should be tuned to get the required quarter wave transformer impedance, which depends on the number of output ports. Besides that, a multi-layer structure technique could be used that is similar to the novel power divider presented in section 3.2 to simplify the structure.

2. Implementing a reconfigurable power divider with in-phase and out of phase reconfigurability feature. The short-ended coupled line quarter wave transformer used in section 3.3 technique could be used to achieve the 180° phase shift between the output ports. Implementing a power divider with a quarter-wave transformer constructed from a coupled line and switching the short end to be open, which can provide a 180° phase shift between the two output ports.

3. Implementing a full duplex system using an array of transmitter more than two antennas. The array could benefit from the technique of equal spacing between the receiver and the transmitter antennas as presented in this work and combining the unequal spacing technique. The feeding network might require a reconfigurable power divider in terms of power ratio and in phase and out of phase configuration. This structure could support the MIMO antenna configuration in full duplex mode.

4. The design principle of power dividers including the antenna array application could be extended to operate in the mmWave bandwidth that represents the new development of 5G mobile generation. The design concepts could be applied to the wafer substrates and integrated on multi-level silicon layers.

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Reconfigurable Wilkinson power divider with unity to 8dB output power differences using one varactor diode

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Abstract

A novel reconfigurable equal to unequal Wilkinson power divider is presented. The proposed power divider adopts coupled microstrip line technique to implement a high impedance section to have unequal output power ratio. A varactor diode is placed between the coupled lines to achieve reconfigurability by changing the reverse biasing voltage on the varactor diode. This enables equal to 8 dB power division ratios between the output ports. A wide range of biasing voltage is used to achieve the smooth power division ratio. A prototype hardware is designed, fabricated and measured to validate the proposed approach. In the equal power division ratio scenario, the measured performance shows a bandwidth of 600 MHz at 5.4 GHz centre frequency. A higher bandwidth of 750 MHz is obtained in the case of unequal power division ratios.

1 Introduction

A Wilkinson power divider with unequal division ratio splits the input power by using two asymmetric quarter-wavelength transformers [1]. In applications where a high power division ratio is required, one of the quarter-wavelength transformers may have a high characteristic impedance, i.e. it becomes a narrow transmission line, which is difficult to implement accurately due to fabrication tolerance. Such a line also suffers from low power handling capacity. Reconfigurable power dividers are used in several applications such as antenna array feeding networks for beamforming [2], diversity applications to obtain a better signal to noise ratio [3] and power amplifier feeds designed to improve efficiency [4]. In addition to the recent work on ultra-wide band power divider by the present authors could also be adopted for possible re-configurability into the future work [5, 6].

To achieve high power division ratio, several novel techniques were presented to realise high impedance microstrip transmission lines, such as defected ground structure [7], offset double-sided parallel strip line [8], coupled lines with two vias [9], coplanar waveguide with electromagnetic band gap [10], applying a groove alongside a high impedance microstrip [11], loading a transmission line with stubs [12] and employing dual transmission lines [13]. None of the mentioned works achieved a continuously variable wide range division ratio except for [14] in which two varactor diodes were placed between the ground plane and a floating potential conductor under the high impedance line. However, the drawback of using defected ground structure is that the ground plane should be kept far from any other electromagnetic materials.

In this letter, a coupled microstrip line is utilized to design a high impedance quarter-wave transformer Wilkinson power divider with unused ends of the coupled lines terminated to the ground. To obtain the reconfigurability, one varactor diode placed at the centre of the loaded short-ended coupled microstrip line that controls the coupling factor and thus controls the coupled microstrip line impedance, which enables varying the output power. A wide bias voltage range for the varactor diode is used to obtain smooth control of the output ports power difference, from equal split to 8 dB.

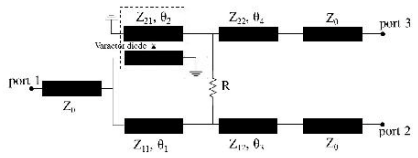

Figure 1. Schematic diagram of the proposed power divider.

2 Power divider design

A 3:1 unequal Wilkinson power divider has been designed using the coupled line technique [9]. Figure 1 shows the schematic diagram of the proposed design. Equations (1–5) [1] are used to calculate the characteristic impedance for the power divider sections. Equations (6-10) are used to approximately calculate the microstrip lines width and length [15]. Referencing [16], the dimensions of the coupled microstrip line can be obtained for the required impedance. In Figure 1 and Equations (1-10) Z_0 represents the divider's input and output ports characteristic impedance, and Z_{ij} represents the characteristic impedances of the power divider sections. R is the value of the isolation resistor. The power division ratio at the output ports 2 and 3 is represented by K^2.

W_{eff}, W and L represent the effective and actual microstrip line width and microstrip line length respectively. The substrate height is denoted by h and the copper thickness by t. The relative permittivity of the substrate material and the microstrip effective permittivity are denoted by ε_r and ε_{eff} respectively. The designed centre frequency is f_0 and λ is the guided wavelength.

The electrical length was designed to be $\lambda/4$ for θ_2, θ_3 and θ_4, while the electrical length for θ_1 is designed to be $3/4\lambda$ as a $\lambda/4$ short ended coupled microstrip line causes a 180° phase shift to the signal it transmits [9]. To compensate that phase shift, an additional 180° electrical length is added to the other section so that the total electrical length become $3/4\lambda$. According to Equation (5), the calculated isolation resistor should be 115.5 Ω and the nearest off - shelf value of 115 Ω was used. The power divider was designed to operate at 5.4 GHz centre frequency to support WiFi applications. The calculated impedances and the optimised dimensions of the proposed power divider are listed in Table 1.

$$Z_{11} = Z_0\sqrt{\frac{1+K^2}{K^3}} \quad (1)$$

$$Z_{21} = K^2 Z_{11} = Z_0\sqrt{K(1+K^2)} \quad (2)$$

$$Z_{12} = Z_0 / K \quad (3)$$

$$Z_{22} = Z_0 K \quad (4)$$

$$R = Z_0\left(\frac{K^2+1}{K}\right) \quad (5)$$

$$Z = \frac{377h}{W_{eff}\sqrt{\varepsilon_r}\left[1+1.735(\varepsilon_r)-0.0724\left(\frac{W_{eff}}{h}\right)^{-0.836}\right]} \quad (6)$$

$$W_{eff} = W + \frac{t}{\pi}\left[\ln\left(\frac{2h}{t}+1\right)\right] \quad (7)$$

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2\sqrt{1+12t/W}} \quad (8)$$

$$\lambda_{eff} = \frac{3*10^8}{f_0\sqrt{\varepsilon_{eff}}} \quad (9)$$

$$L = \lambda_{eff}/4 \quad (10)$$

	Value (Ω)	Width (mm)	Length (mm)
Input / output ports	50	1.84	8.47
Z_{11}	43.9	2.26	25.18
Z_{12}	28.9	4.1	8.16
Z_{21}	131.6	0.125	9.31
Z_{22}	86.6	0.63	8.84

Table 1. Proposed power divider design parameters.

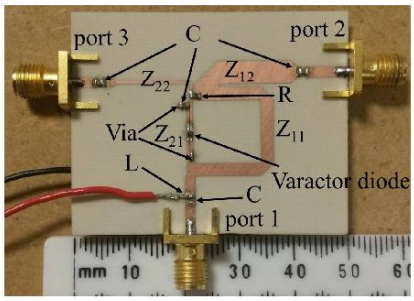

Figure 2. Photograph of the fabricated reconfigurable power divider.

The high impedance section Z_{21} is constructed by using a microstrip coupled line with a coupling factor of 0.3 and terminating the open ends to the ground. The calculated spacing between the coupled lines is 0.49mm. A varactor diode connected between the coupled lines achieves the low odd-mode impedance needed for tight coupling [17]. In accordance with this, the coupled line width and the spacing between them were recalculated taking into consideration the presence of the varactor diode. The new width and spacing between the coupled lines were found to be 0.4 mm and 0.108 mm respectively.

Rogers RO4003C substrate with a dielectric constant of 3.38 and a thickness of 0.813 mm was used to fabricate the proposed power divider. Figure 2 shows the fabricated prototype with an overall dimension of 50 × 40 mm. To bias the varactor diode, a choke inductor L of 96 nH was used to isolate the RF signal from the DC source and blocking capacitors C of 850 pf were placed at the input and the output ports to isolate the DC voltage from the vector network analyser. A silicon junction varactor diode from Skyworks (SMV1231) is used between the coupled lines. Changing the varactor reverse bias from 0 to 15 V changes its equivalent capacitance from 0.4 to 2.1 pf. This corresponds to an output ports power difference ranging from 8.25 to -1.16 dB as shown in Figure 3. The DC power consumption of the biasing circuit with the varactor diode is negligible.

3 Experimental results

The proposed unequal power divider was designed to work at 5.4 GHz for WiFi applications. Figure 4 shows measured performance for a 6 dB output ports power difference, which required a varactor reverse bias of 4.4 V. The input port return loss is better than 10 dB for a bandwidth of 750 MHz ranging from 5 to 5.75 GHz and the insertion loss from the input to ports 2 and 3 is 5.6 and 11.8 dB respectively at 5.5 GHz. The amplitude imbalance for a 40 MHz WiFi channel within the operational band of 750 MHz is below ± 0.1 dB.

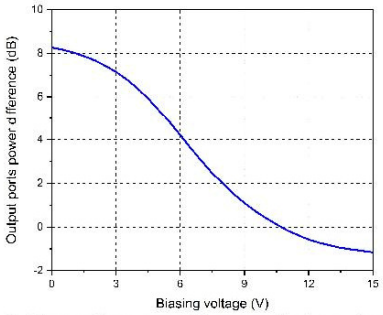

Figure 3. Measured response with reverse biasing voltage.

A 1 V reverse bias is applied to the varactor diode to achieve the 8 dB output ports power difference case. The divider performance in this case is shown in Figure 5. It is observed that the input port return loss bandwidth is 1 GHz from 4.75 GHz to 5.75 GHz. The insertion losses to ports 2 and 3 are 5.6 and 13.5 dB respectively at 5.5 GHz. The amplitude imbalance for the 40 MHz WiFi channels is also below ± 0.1 dB.

For the case of equal output ports powers, a 10.4 V reverse bias is applied across the varactor diode. A return loss better than 10 dB for a bandwidth of 600 MHz from 5.1 GHz to 5.75 GHz is shown in Figure 6. It is clear that both output ports have an equal insertion loss of 6.7 dB at 5.5 GHz. The amplitude imbalance in this case for the 40 MHz WiFi channels is ± 0.2 dB. A slight difference can be observed from Figure 3 to Figure 5, which is due to simulating the tuning elements as ideal lumped elements.

Figure 3 shows that the proposed power divider has a wide control range of 9.4 V, which helps to achieve more precise division ratios using a single varactor diode for a normal 5 GHz WiFi system which will distinguish between 42 channels. The work presented in [14], used two varactor diodes to achieve a reconfigurable division ratio between 2 and 10 dB by changing the biasing voltage over a smaller range from 2 to 4 V. For this reason, the current work is considered to be better in terms of using fewer varactor diodes, having less critical tuning, and being easier to implement. It is believed to be less affected by a metallic enclosure as compared to reported works.

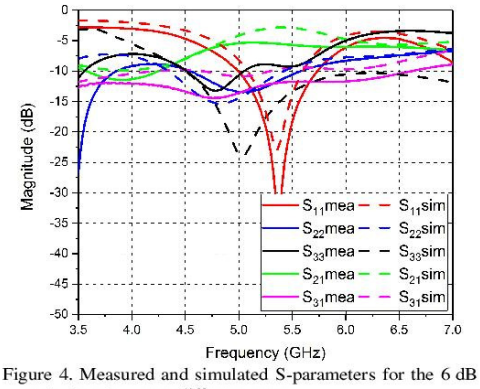

Figure 4. Measured and simulated S-parameters for the 6 dB output ports power difference case.

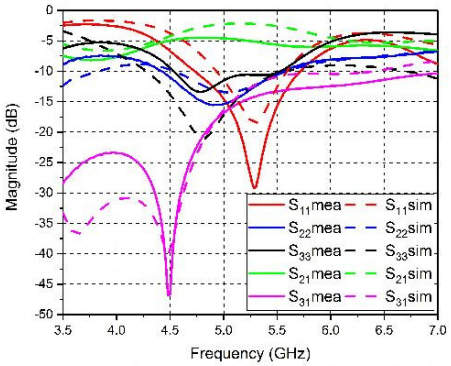

Figure 5. Measured and simulated S-parameters for the 8 dB output ports power difference case.

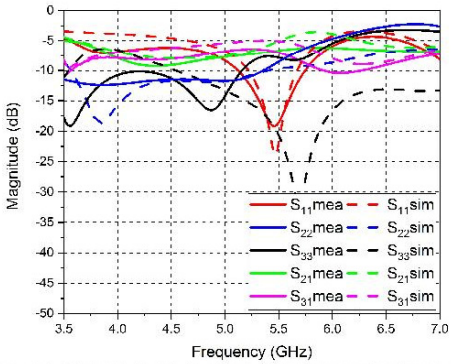

Figure 6. Measured and simulated S-parameters for the equal output ports power case.

4 Conclusion

A novel reconfigurable Wilkinson power divider has been presented. The power divider configuration employs parallel-coupled microstrip line for the high impedance quarter wave transformer section. The proposed power divider can obtain an 8 dB to unity power division ratio between the output ports using only one varactor diode, by applying a reverse bias voltage ranging from 1 to 10.4 V. A good amplitude imbalance is achieved between the output ports which was below ± 0.1 dB and ± 0.2 dB for the unequal and equal division cases respectively. To verify these results, a prototype was developed and tested. The measured performance has good agreement with simulation and is suited to operation at 5.4 GHz for Wi-Fi applications.

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A general design for multi-output ports planar Wilkinson power divider

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Abstract
A general design for a microstrip-fed multi-output port planar Wilkinson power divider is proposed, designed and fabricated for industrial, scientific and medical radio band applications. The realized design operates in a wideband frequency range from 1.77 to 2.88 GHz with a low insertion loss imbalance below 0.01 dB at 2.4 GHz. The power divider adopts a two-layered structure and microstrip feeding, thus solving the isolation resistor interconnection crossover problem for dividers with more than two output ports. A one-section quarter wave transformer is employed on the upper layer and the second layer is used to interconnect isolation resistors between the output ports. Two different permittivity substrates are chosen to simplify the designed structure. A prototype of a one to five ports power divider has been selected as a design example and fabricated. The measured scattering parameters agree well with simulation, which validates the design.

Keywords: Wilkinson Power divider, Multi-output, Planar structure, Microstrip feeding.

1 Introduction

Power dividers are vital components in electromagnetic circuits, typically providing three matched ports using transmission lines where each line has an electrical length of a quarter wavelength at a designed center frequency [1]. The earliest power divider with high output port isolation was reported by E. J. Wilkinson in 1960 and was named after him. He improved the output port isolation of a T-junction power divider by introducing a resistor between those ports. Later on, the Wilkinson power divider has been extensively studied and developed for multiple applications such as antenna array and power amplifier feeding networks, mixers, and modulators. These applications often require a divider with multiple output ports to divide and combine microwave signals between multiple system elements.

However, for layouts with more than two output ports, Wilkinson power dividers are not easy to implement as a planar structure since the isolation resistors need to be connected in a star configuration so that they require crossovers. This makes it difficult to implement single stage planar structures. Many studies have reported methods to overcome this problem. The commonest method is by implementing several cascaded stages [2] but few

of these designs have been successful in implementing a planar structure [3]. However, power dividers with cascaded stage structures will suffer from greater conductor losses, due to greater overall transmission line lengths, and sometimes amplitude imbalance. To overcome these problems, a planar power divider is proposed in which isolation resistors with their interconnections are implemented on an additional layer. The presented design has a simple structure utilizing microstrip feeding ports. In this paper, a design procedure for an N-way planar Wilkinson power divider is presented and validated by prototype fabrication and measurement.

2 Power Divider Design

The block diagram for a general Wilkinson power divider with N output ports is shown in Figure 1. It shows the isolation resistors connected in a star configuration. A power divider with two output ports does not suffer from a problem in connecting the isolation resistor, as only one is needed. The quarter wavelength transformers are separated at the output end by a small space that is usually kept a small fraction of the wavelength (λ) to ensure better input and output ports return loss and output ports isolation. However, transmission lines have a $\lambda/2$ periodicity phenomenon. The terminating impedance is transformed to the same value for every added length of $\lambda/2$ [1]. Thus, a line with a length of $\lambda/2$ and its multiples can be used to connect isolation resistors between separated output ports.

In order to achieve a single section planar power divider with more than two output ports, a two-layered substrate has been used. The input and output ports with quarter wave transformers are designed to be on the upper layer, whilst the resistors with their microstrip line interconnections are implemented on the lower layer. A common ground plane separates these two layers and vias are used to connect the resistor section with the intersection point of each $\lambda/4$ transformer and output port as shown in Figure 2.

The characteristic impedance of input and output ports is represented by Z_0 in Figure 1, while $Z_{\lambda/4}$ represents the quarter wave transformer impedance, R represents the isolation resistor. The microstrip line connecting the isolation resistors impedance value is represented by $Z_{\lambda/2}$. To prove the concept, a five-output ports power divider is selected as a study case. The values for $Z_{\lambda/4}$ and R are calculated using equations (1-2) [4]:

$$Z_{\lambda/4} = \sqrt{N} Z_0 \tag{1}$$

$$R = Z_0 \tag{2}$$

The input port, quarter wave transformer and output ports width and length can be calculated approximately by using equations (3-7). In these equations, h represents the substrate height in mm, t represents the copper thickness in μm and W and L represent the microstrip line width and length respectively in mm; ε_r and ε_{eff} represent the actual dielectric constant and the effective dielectric constant respectively. The equations below are subject to W/h< 1[1]:

$$Z = \frac{87}{\sqrt{\varepsilon_r + 1.41}} ln\left(\frac{5.98h}{0.8W + t}\right) \quad (3)$$

$$W = \frac{7.48h}{e^{\frac{Z\sqrt{\varepsilon_r + 1.41}}{87}}} \quad (4)$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + \frac{12h}{W}}} \quad (5)$$

$$\lambda_{eff} = \frac{3 \times 10^8}{f_0 \sqrt{\varepsilon_{eff}}} \quad (6)$$

$$L = \lambda_{eff}/4 \quad (7)$$

The optimized values for the design parameters are listed in Table 1. The SMD resistor (R) size selected to be 0402 with a value of 50 Ω. The fabricated planar Wilkinson power divider is shown in Figure 2. The first layer implemented on a 0.51 mm thick RO5880 substrate with a dielectric constant of 2.2 and the bottom layer implemented on a 1.28 mm thick RO3010 substrate with a dielectric constant of 10.2. The copper thickness for both substrates is 17.5 µm. The resistors interconnection microstrip lines width and vias diameter can be selected arbitrarily.

The upper layer substrate dielectric constant is selected to be less than the lower layer substrate dielectric constant in such a way that the physical length of the λ/2 microstrip lines connecting the resistors, with the chosen substrate thicknesses, is equal to the physical length of the λ/4 transformers. This allows construction of short and straight microstrip lines for the isolation resistors interconnection. An arbitrary impedance can be selected for those lines, as its value does not greatly affect the results, as has been validated by a parametric study. The proposed power divider dimensions are 97 × 72 mm. The lower substrate is cut to a size of 58 × 36 mm, simply to allow space for soldering the SMA connectors.

Although a similar concept has been reported in [4], in that work a more complicated design was needed and a more complex fabrication procedure was used. A coaxial feeding port was used that was soldered on the ground layer between the two substrates, and this required drilling of the central part of the lower layer to allow placement of the coaxial connector. In contrast to that difficult to implement the previous feeding method, a microstrip line is used here and this makes the design more suitable for planar structure applications. In addition, an impedance matching disk was required in the previous work to feed the λ/4 sections and so obtain a better input port matching. Here the λ/4 sections are directly connected to the input ports without the need to introduce additional structure. In addition, by using microstrip feeding the number of drilled via holes was reduced.

Moreover, an Archimedean spiral line was used for the isolation resistor interconnection in the previous work, which requires more complex design calculations. Using the straight microstrip lines benefits from using higher permittivity substrate for the isolation resistors interconnection layer. In the earlier work, a microstrip ring was placed on the lower layer

around the coaxial connector and was needed for interconnecting the isolation resistors due to the central position of the connector. In the present design, isolation resistors are connected directly without the need for additional structure. In [4], the same concept as [5] has been used but implemented for dual-band operation.

3 Experimental Results

Input and output port return losses are shown in Figure 3. It is clear that the power divider covers a wide bandwidth of 1.11 GHz from 1.77 to 2.88 GHz with a return loss of 25.5 dB at 2.4 GHz while maintaining the return loss below 10 dB over the operational band. All output ports return losses are about 18 dB at 2.4 GHz and below 15 dB for the operational band. The isolation performance between output ports is better than 25 dB at 2.4 GHz and is maintained below 20 dB over the whole band as shown in Figure 4. The measured insertion loss at 2.4 GHz is 7.4 dB compared to a 6.99 dB theoretical ideal value. The amplitude imbalance is less than 0.01 dB at 2.4 GHz as shown in Figure 5, becoming ±0.3 dB near the lower and upper band edges. In order to simplify figures, only three ports have been selected which are the input port (port one) and two output ports (ports two and three) to show power divider performance and compare the measured and the simulated results; these are in good agreement.

4 Parametric Study

Two parametric studies have been carried out to study the effect on the performance of changing the width of the microstrip lines connecting the resistors ($Z_{\lambda/2}$) and the diameter of the vias.

A range from 0.8 to 1.2 mm was selected for the width with an increment of 0.2 mm. Figure 6 shows the power divider performance for each case. It is clear that the resistor interconnecting microstrip line width does not have a noticeable effect on the performance; the input and output ports return losses and isolation between output ports are slightly changed but the effect is practically negligible. For this reason, an arbitrary width can be selected. In this design, the width is selected as 1 mm to facilitate soldering of the SMD resistors.

Similar behaviour for the power divider performance can be observed in Figure 7 when changing the via diameter from 0.8 to 1.2 mm with an increment of 0.2 mm. This shows that the via diameter does not discernibly affect the power divider performance. A mechanically convenient diameter of 0.8 mm was selected.

It is observed that the power divider performance is not affected by changing the microstrip line width connecting the isolation resistors as shown in Figure 6, and the via diameter as shown in Figure 7, due to the l/2 line holds identity length at the exact centre frequency regardless of the line impedance. This suggests impedance will be not very critical over the 48% relative spectrum bandwidth.

5 Conclusions

A five-way planar power divider has been designed as an example of a general N-way planar Wilkinson power divider. To overcome the isolation resistor crossover problem when N>3, a third layer has been introduced. To make the design and fabrication procedure easier, a microstrip feeding method has been selected. The permittivity of the lower layer substrate is selected to be higher than the upper layer substrate in such a way that the quarter wave transformer physical length equals the physical length of the electrically half - wavelength microstrip lines interconnecting the isolation resistors. The proposed design reduces the need for cascading a number of sections, which reduces the conductor losses and hence the total insertion loss. The resistor interconnection line width and the via diameter were shown by the parametric study to be arbitrarily selectable as they have a negligible effect on the power divider performance. The practical measurements agree well with simulation results and validate the design concept. The wideband operation, very good isolation and insertion loss, with very good amplitude balance, make this power divider well suited for industrial, scientific and medical radio band applications.

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A simple self-interference cancellation technique for full duplex communication

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Abstract— Recently, a considerable attention has been paid for full duplex communication. Full duplex allows transmitting and receiving at same frequency simultaneously. As a result, the spectral efficiency can be increased two times by utilizing this type of communication. Nevertheless, the substantial issue of applying full duplex communication is the self-interference signal. This paper presents a new method of antenna cancellation with symmetric antenna placements to cancel the self-interference signal. Three monopoles antennas are modelled by using Computer Simulation Technology (CST) program; one as a receive antenna, while others as transmit antennas. The cancellation of the method is calculated by utilizing Matlab code. Moreover, many factors that could degrade the system performance are investigated. Results illustrate that this technique provides higher than 50 dB cancellation in a typical situation. However, results show a decline in the efficiency of the technique when there is an inaccuracy of placing the antennas, or amplitude mismatch between two transmitted signals. The obtained simulation results are verified by testing the technique practically. The results show that the practical prototype can provide more than 40dB cancellation over a wide band frequency.

Keywords: Full Duplex Communication; Self-Interference Signal; Antenna Cancellation with Symmetric Antenna Placements; Analogue Cancellation, Digital Cancellation.

I. INTRODUCTION

Existing wireless networks are basically using half duplex mode on a single channel. In this mode, systems can send and receive on different times or frequencies to avoid the interference between the two signals. Frequency Division Duplex (FDD) and Time Division Duplex (TDD) are the two main techniques of half duplex mode, which are exploited in the current wireless systems [1]. Even though TDD and FDD improve communication systems, both techniques cannot be used to receive and transmit concurrently over an entire bandwidth that is assigned for a system [2].

Recently, the massive proliferation of wireless networks causes a spectrum shortage of the frequency band that has been assigned for wireless communication networks [3]. Therefore, there has been a considerable concern about full duplex mode to be the future direction of wireless systems [3-4]. Full duplex communication means a system can transmit and receive on the same frequency at the same time. Consequently, the spectral efficiency will be theoretically twofold. In addition, it can solve some problems, such as large end-to-end delays and eliminating hidden terminal issue [5].

The associated problem that prevents the fulfilment of a practical full duplex mode is the self-interference signal. This signal is generated by the transmit antenna of the same node, and it is received by the receive antenna with the desired signal that comes from different node [3]. Because of the space between the receive antenna and transmit antenna is so small comparing with the distance between two nodes, the power of self-interference signal is approximately 100 dB higher than the desired signal [6].

In spite of the fact that original signal can be recognized and simply removed at a receive chain, it is hard to do that. Actually, radios do not know what they are sending. In other words, radios can only identify the pure digital baseband signal, and cannot distinguish the signal after converting it to analogue form, and carrying it by a carrier frequency [7].

The concern about cancelling the self-interference signal has been rising recently. Many methods have been suggested in order to cancel or reduce the self-interference signal. These techniques are categorized into three main groups: digital, analogue and antenna cancellation [5].

In this paper, a new method of antenna cancellation with symmetric antenna placements is proposed to reduce the self-interference signal [8]. The CST software is used to model the technique, which consists of three monopoles antennas, one as a receive antenna, whereas others as transmit antennas. Additionally, a code in Matlab is utilized to calculate the cancellation performance. Finally, the proposed method is tested practically.

II. SELF INTERFERENCE CANCELLATION TECHNUIQES

- **Antenna cancellation**: This technique is simply achieved by using more than one transmit or receive antenna, and it could be multiple transmit and receive antennas. These

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antennas are structured in such a way to force the transmitted signals to cancel each other at the receiving antenna [9].

In [5], antenna cancellation with asymmetrical antenna placement has been presented. The design consists of three antennas, two as transmitters, while the other one as a receiver which is placed between the two transmitters. The distance between the first transmit antenna and the receiver is d, whereas the second transmit antenna is placed at distance d+ (λ/2) away from the receiver. The aim of adding an extra distance (λ/2) for the second transmit antenna is to make the second transmitted signal crosses extra distance (λ/2) to reach the receiver than the first transmitted one. As a result, there will be 180^0 phase difference between them, and will eventually cancel each other at the receive antenna. This method can reduce the self-interference signal by up to 30dB [8].

The method in [5] has a limitation in terms of bandwidth and size. Firstly, the suggested idea relies on placing one transmitter by an extra distance (λ/2) to destruct the two transmitted signals at the receiver. The wavelength is obviously calculated from a single frequency. Consequently, the design will work perfectly at the frequency which has been used to find λ, and the performance will degrade when moving away from that frequency. Thus the system cannot provide high and stable cancellation over a wide frequency band. Additionally, adding extra (λ/2) distance will produce larger antenna structure that could not be fixed at wireless devices. For instance, at 2.4 GHz frequency, this design needs 7 inches, which will not be fit in some devices, such as access point and laptop body.

Antenna cancellation with a symmetric antenna placement has been proposed in [10] for which two transmit antennas with one receiver are utilized. The distances between transmit antennas and the receive antenna are equal. The original signal is divided into two symmetric signals in amplitude and phase. One of these two signals is connected to one transmit antenna directly, while the other signal passes through a 180^0 phase shifter. Therefore, the two signals will arrive at the receiver with 180^0 phase difference, and will be added destructively. Comparing this technique to the method in [5], this design has many benefits. Firstly, the idea of using a phase shifter to create the phase difference instead of adding extra distance to one of the transmit antennas, leads to providing high cancellation on a wider band frequency than on a single frequency. Secondly, because of the two transmit antennas are separated on equal distances from the receive antenna, studying channel behaviour and its effects on the transmitted signals are not required, because the impact will be the same at the two signals. Nevertheless, the insertion loss of the phase shifter must be compensated in the other signal path, and the frequency response of the phase shifter is not flat over a wide bandwidth.

- **Analogue cancellation:** this idea is based on using the transmitted signal at the receive chain, because the transmit chain is close to the receive chain. Therefore, copy of the sending signal can be taken, and subtracted from, or added to the received signal. This process is achieved before the Low Noise Amplifier (LNA) in the RF domain [9].

Balanced/unbalanced (Balun) transformer with two antennas are utilized in [12]. In addition, an automatic circuit is applied. The transmitted signal is divided into two signals, that are similar in amplitude but with 180^o phase difference between them. The transmitter is fed by one of these two signals for sending, whereas the second signal (the inverted one) is connected to the input of the tuning circuit. The goal of implementing the tuning circuit is to adapt and modify the phase and the amplitude of the inverted signal quickly, automatically and accurately, according to the second input of the tuning circuit, which is the received signal. After that, the inverted signal will be added to the received signal to reduce the effect of the self-interference signal. Measurements show that this technique provides 45dB cancellation over 40 MHz bandwidth. However, it has some limitations. For example, due to the inaccuracy of manufacturing, balun transformer could suffer from leakage or non-flat frequency response issue. Additionally, effects of the channel on the sending signal are ambiguous and not easy to compensate them.

In [12], single antenna with a circulator is suggested to cancel or reduce the self-interference signal. The antenna is used for sending and receiving, and the circulator to isolate these two signals. Therefore, there is no self-interference signal composited with the received signal. However, the circulator has a leaking problem between its ports. Hence the port of the sending signal passes part of the signal to the port of the received signal. Results indicate that this design can provide around 75dB cancelation on 10MHz bandwidth.

Using noise canceler chip for cancelling the self-interference signal is presented in [13]. It is known as QHx220. This chip can supply extra 20dB cancellation, when it is added with other cancellation methods, such as antenna and digital cancellation. Nevertheless, negative influences could be added to the received signal; for example, distortion and non-linearities. As a result, implementing digital cancelation stage after this chip will be very complicated.

- **Digital cancellation:** at this stage, the generated baseband signal at the transmitter is subtracted or added to the output of the Analogue-to-Digital Converter (ADC) at the receive chain. Memory is utilized to store transmit digital samples. After that, the amplitude and phase of these samples are modified to be similar or opposite to the sending samples which exist at the received signal. Then, the subtraction will be applied between the adjusted samples and the received samples to remove the residual self-interference signal [9].

III. ANTENNA CANCELLATION DESIGN

This section analyses the method of antenna cancellation with symmetrical antenna placements. In this technique, three monopole antennas are implemented, two as transmit antennas, while the other as a receive antenna. A hybrid junction is used to supply the required 180° phase instead of the phase shifter [8]. The use of the hybrid circuit offers two output signals of equal amplitudes thus the problem of unequal amplitudes caused by the attenuation of the phase shifter [10] is solved. Moreover, any ripple in the frequency response of the phase shifter degrades the cancellation since it affects one of the two transmitted signal. On the contrary, ripples in the hybrid circuit response affect both signals and leading to better cancellation across a wider frequency band.

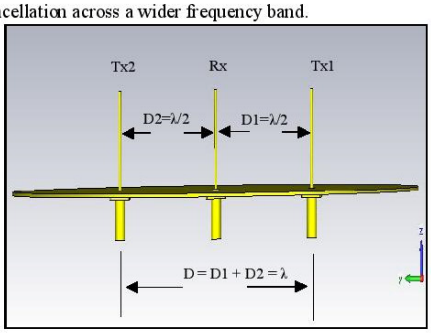

Fig. 1. Model of antenna cancellation with symmetric antenna placements.

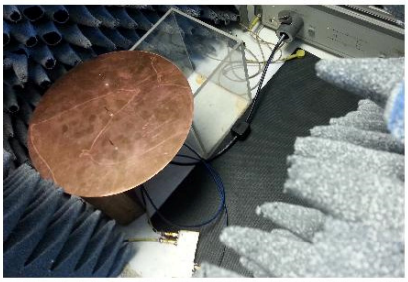

Fig. 2. Practical design of a symmetrical antenna cancellation method.

The two transmitters are placed at equal distances from the receiver. As shown in figure 1, the receiver is located between the two transmit antennas, and it is separated by ($\lambda/2$) from each transmitter. The two transmitters are fed by the outputs of a hybrid junction which supplies two output signals of equal amplitudes and 180° phase difference. Consequently, the signals from the two transmitters will cross equal distances and reach the receiving antenna and cancel each other. The occupied space by this prototype is one wavelength (D1 + D2 = $\lambda/2 + \lambda/2 = \lambda$ = 12.449) cm at frequency of 2.45 GHz.

This method provides higher cancellation over a wide band frequency. There are two reasons behind that. Firstly, the distance between antennas is similar. Secondly, a hybrid junction can create two signals similar in amplitude with 180° phase difference over a wide band frequency. Therefore, high self-interference cancellation over a wider band frequency can be obtained by using this technique.

After the introduction of a second transmitting antenna, then the total signal at the receiver is the sum of the (V_1) due to the first antenna and ($aV_1e^{-j\phi}$) due to the second antenna, where the symbol (a) accounts for attenuation and (ϕ) is the phase shift in the hybrid junction. The reduction factor RF can be defined by the ratio of the received power with one transmitting antenna and that with two receiving antennas:

$$RF = [V_1 / (V_1 + aV_1e^{-j\phi})]^2 \quad (1)$$

$$RF = 1 / [(1+a\cos\phi)^2 + a^2\sin^2\phi] \quad (2)$$

This factor approaches infinity for the ideal case (a=1, and ϕ=180°), while the worst case value is 0.25 or -6dB when (a=1 and ϕ=0). For a desired reduction factor RF=X dBs, then the values of a and ϕ will be related by:

$$RF = 1 / [1 + a^2 + 2a\cos\phi] = 10^{0.1X} \quad (3)$$

which can be reduced to:

$$1 + a^2 + 2a\cos\phi = 10^{-0.1X} \quad (4)$$

When a=1, then the allowable phase deviation $\Delta\phi$ from 180° should be:

$$\cos(\Delta\phi) = 1 - 0.5 \times 10^{-0.1X} \quad (5)$$

As example for 20 dB reduction, then $\Delta\phi$=5.73°.

A code in Matlab was written to verify the idea of antenna cancellation, and calculate the reduction factor that represents the performance of cancelling the self-interference signal. The Matlab code utilizes the S parameters that are obtained from the CST program to check the cancellation performance under the following conditions:

a. An ideal case; with no phase error and matched devices.
b. Certain error such as placing antennas in inaccurate position.
c. Mismatch between the two sending signals in terms of phase and amplitude.
d. Operation over a wide frequency range

IV. IMPLEMENTATION OF ANTENNA CANCELLATION

The suggested model was implemented practically, with three monopoles antennas which were fixed on a circular copper plate as shown in Fig. 2 [8].

V. SIMULATED AND PRACTICAL RESULTS

In this section, the simulated results of the model that are obtained by running Matlab and CST programs are displayed

and discussed. Additionally, it displays and discusses results of the implemented model.

Figures 3 shows the reflection coefficient of the receiver antenna (S_{11}), the reflection coefficient of first transmitter (S_{22}) and reflection coefficient of second transmit antenna (S_{33}). The reflection coefficients S_{11}, S_{22} and S_{33} are below -20dB across the band with a minimum of -30dB at 2.45GHz. Thus, the prototype fulfils the (802.11b/g/n) band (Wi-Fi band). Additionally, the values of S_{12}, S_{21}, S_{23} and S_{32} are equal, because the three antennas are identical, and the similarity in distances between the two transmitters and the receiver, which leads to equal channel attenuation on both forward transmission gains (S_{21} and S_{31}). Consequently, there is no need to study channel behaviour by using this technique. The values of S_{21} and S_{31} are approximately -14dB at 2.45GHz, these two values can be reduced by increasing the distance between the antennas, which leads to increase the cancellation performance. However, the size of the model will be larger.

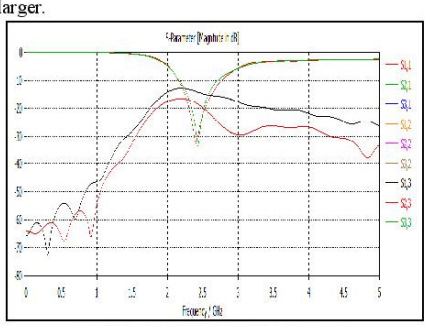

Fig. 3: S parameters of the simulated model.

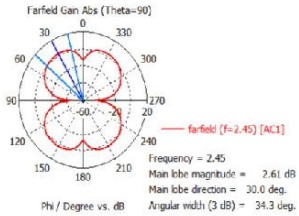

Fig. 4: Far field radiation pattern.

Figures 4 illustrates the far field radiation pattern of the model. It can be seen that two nulls at the far field are produced, due to the 180° phase shift between the two transmitters which forms an endfire array. While using two transmitting antennas can offer good cancellation by placing a null in the direction of the receiving antenna, the two transmitting antennas obviously have radiation pattern that is different from that of a single one. Two transmitting antennas with phase shift of 180° means an endfire array whose null is along the array axis. However, the presence of the receiving antennas modifies the pattern to the one shown in Fig. 4. There is a deep null in the direction normal to the axis of the three antennas. Therefore, the coverage of this arrangement is different from that of a single monopole antenna.

Figure 5 shows the cancelation performance of this technique versus phase angle and frequency. It is obvious that this method produces high cancellation (around 50dB). The frequency response of the proposed method is limited by that of the hybrid circuit and the used antennas. Thus, this method can offer much wider band than the methods based on the phase shift that is caused by separating distances or phase shifters.

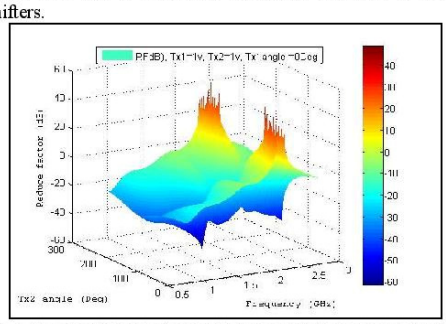

Fig. 5. Model performance of cancelling the self-interference signal at perfect conditions.

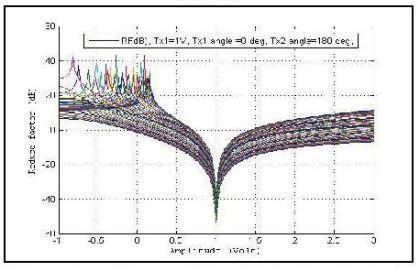

Fig. 6. Cancellation performance of the model when the amplitude of Tx2 is varied while the amplitude of Tx1 is fixed to 1V.

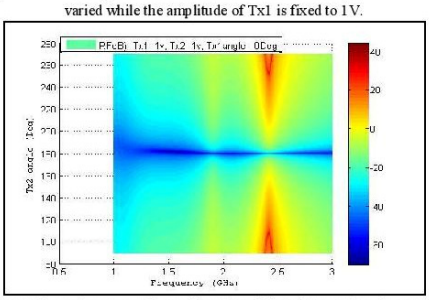

Fig.7: The performance of cancelling the self-interference signal over the frequency range 1-3 GHz.

Figures 6-7 show the cancellation performance when the amplitude of the (Tx1) is fixed to 1v, and the amplitude of the

(Tx2) was varied. It can be seen that highest cancellation can be achieved when the voltage of the two transmitted signals are equal.

Figure 8 shows the impact of error in the 180^0 phase difference between the two sending signals. Such error can occur in the splitter circuit or in the position of the two transmitters.

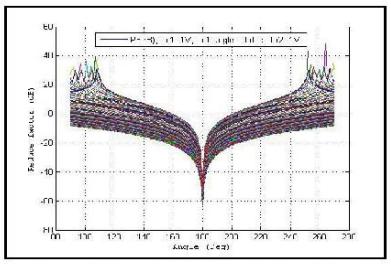

Fig. 8. The cancellation performance when the phase deviates from 180^0.

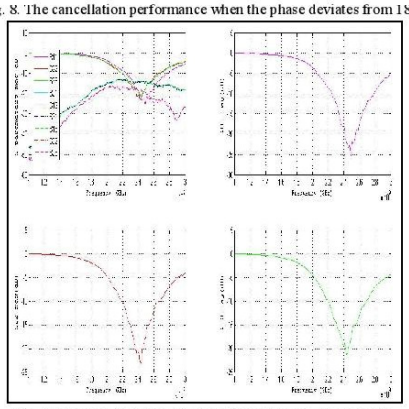

Fig. 9. S-parameters, S11, S22 and S33 of the practical model.

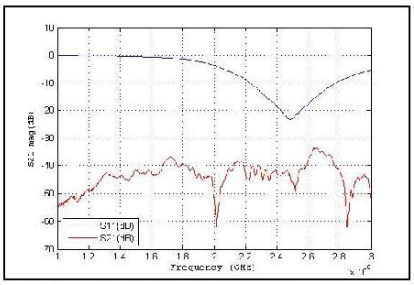

Fig. 10. The performance of practical model for cancelling the self-interference signal.

Figure 9 shows S-parameters of the practical model [7]. It can be noted that S parameters of CST model and S parameters of the design are quite close.

Figure 10-11 display the cancellation performance over a wide band frequency, it is symbolized by S_{21} in the two figures. It is clear that the value of S_{21} is -45dB across the range (2.2GHz-2.8GHz), when the power of the sending signal is -5dB. Which means that the design provides 40dB cancelation over a wider band frequency (24%).

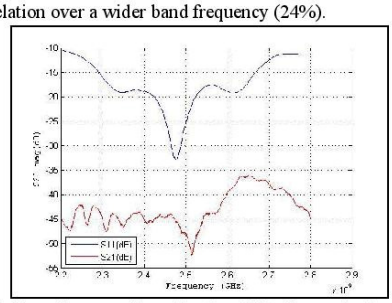

Fig. 11. The performance of cancelling the self-interference signal across the range (2.2GHz-2.8GHz).

VI. CONCLUSIONS

Antenna cancellation with symmetric antenna placement technique to cancel the self-interference signal has been presented. The idea is based on placing two transmitting antennas at similar distances far from the receiving one. A hybrid circuit is used to supply the 180^o phase shift. The model was designed to work on 2.45GHz. CST program was used to model the prototype, and obtaining S-parameters of the model. Matlab code was written to find the cancelation performance of the prototype.

The results showed that in perfect conditions, this technique provides more than 53dB cancelation over a wider bandwidth. Additionally, results also demonstrated that the amplitude mismatch and the inaccuracy of placing antennas in their right positions, lead to degrading in the cancelation performance. The practical design of this method achieves higher than 40dB cancelation over a wider bandwidth (24%).

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Reconfigurable Design Model of Bow-Tie Dipole Adjacent Lossy Dielectric Using Optimisation Method in Hybrid Electromagnetic Technique

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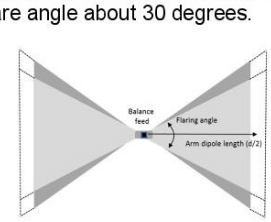
The optimization of Bowtie antenna next to lossy dielectric rectangular volume shown in Fig. 1 is simulated and studied to achieve stable frequency response over a wide range. The dielectric has dimensions 1.25λ (the wavelength is corresponding to the centre frequency 2.5 GHz), 0.833λ and 1.66λ, with ε_r = 52, σ = 0.85 inserted into the total field region of the hybrid domain. The separation distance 'd' between the dipole and the dielectric was varied over three values; these are 10, 20 and 30 mm. This problem was simulated using hybrid MoM/FDTD [1]. The antenna design was optimised using the FireFly algorithm [2]. Details of all methods were demonstrated in Table 1. The Hygence surface that encloses the dielectric material was modelled using a number of cubical cells equal to 58×42×74 (the cell size is equivalent to 0.025λ, that is 3 mm). We have set up three cases for the flare angle and then optimised the length arm of the Bowtie antenna for distances from the dielectric volume. It is aimed to achieve the matching over a wide bandwidth around 2.5 GHz. Therefore the fitness function for the FF algorithms was covered by few frequencies components that possible to meet the best matching at the port of the antenna. The cumulative function for case 3 at 30 mm is shown in Fig. 2 with good convergence rate to optimum solution. The return loss for various lengths of antenna arm (d/2) was illustrated into the Fig. 3 for the case 1. It is quite clear a bandwidth of around 1750 MHz can be achieved for few arm lengths as optimised clearly for flare angle about 30 degrees.



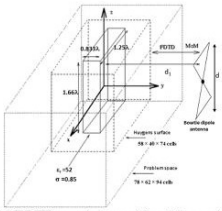


Fig. 1a Basis geometry for the Bowtie antenna, Fig. 1b Hybrid MoM/FDTD model used for this work..

Table 1. Input MoM, FDTD and FF parameters of Example 2.**FDTD parameters**

Formulation	Total/scattered field
Operating frequencies	1.5, 2.5, 3 GHz
px, py, pz	58,42,74
mx, my, mz	78,62,94
Total number of FDTD cells	77×61×93 = 436821
nlayer	8
Δ	0.003
Δt	4 ps
Time cycles	25
ax, ay, az	17,17,23
xmin, xmax	*nlayer*+6, mx-*nlayer*-6
ymin, ymax	*nlayer*+6, my-*nlayer*-6
zmin, zmax	*nlayer*+6, my-*nlayer*-6
Huygens surface size (S_c) mm	174 × 126 × 222
MoM parameters: Bowtie antenna	
flare angle: Case 1: 25 to 35, Case 2: 45 to 55, Case 3: 55 to 65	
d1: Case 1: 10 mm, Case 2: 20 mm, Case 3: 30 mm	
Length (d/2)	15 mm to 30 mm
The **FF method** is characterized by the following: Max gen = 100, γ = 1, npop, 20, βmin = 0.2 and α = 0.5.	

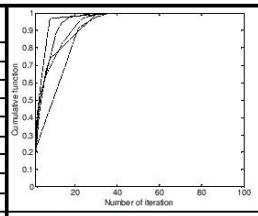


Fig. 2, Case 3 at d1 = 3 cm for 5 attempts of the FF algorithm; variations of cumulative function.

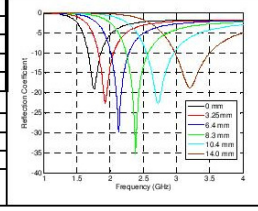


Fig. 3 Return loss at the input port for different cuts distances from the edge of the antenna arm.

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An Ultra Wide Band Power Divider for Antenna Array Feeding Network

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***Abstract*—This paper presents a design procedure for a physically small, equal phase and equal power, 1-to-4 ultra-wideband Wilkinson power divider is presented. Initially, a 1-to-2 divider was designed and optimized for the full 3.1 GHz to 10.6 GHz range. The 1-to-4 divider was realized using three 1 to 2 dividers, and further optimized for full band insertion loss, return loss, and isolation. The circuits were constructed using a 0.75mm thick Rogers RO3035 substrate, and experimentally validated.**

Keywords— antenna array feeding, ultra wideband (UWB), small size power divider

I. INTRODUCTION

A Wilkinson splitter is a three port matched transmission line device which is designed to operate at a frequency where the phase length of the unit element is one quarter wavelength. The original design concept, due to E.J.Wilkinson, was reported in 1960 [1]. Wilkinson was able to improve the isolation between the two outputs, and improve the return loss of a T-junction power divider by the introduction of an isolation resistor. This class of hybrid splitter is essentially a narrowband device, and several methods have been developed for increasing the feasible operating bandwidth. Such methods include the addition of new sections [2], the addition of stubs to each section [3-5], and the use of a slotted ground plane [6]. Commercial UWB (3.1 GHz – 10.6 GHz) sub-system applications [7], including antenna arrays, are increasingly commonplace. Thus, any such divider must satisfy the enhanced bandwidth requirement, whilst maintaining a constant insertion loss and a good level of isolation between the output ports [8].

II. DESIGN CONCEPT AND PROCEDURE

The first step is to design a 2-port splitter which should be optimized for the full operational bandwidth – in this case from 3.1 GHz to 10.6 GHz. Then three such dividers are combined to construct a two-stage 4-port splitter. Single section Wilkinson dividers consist of two 70 Ω quarter wave transformers terminated by a 100Ω resistor [9]. To expand the working bandwidth, it is possible to add further quarter wavelength transformers. These transformers are also terminated with resistors with different values[10]. By referring to look-up tables and charts, the design parameters for these transformers and resistors can be obtained [9-11].

The initial design values for the section impedances, and resistors, used in the paper are listed in Table 1. The circuits were fabricated using a 0.75 mm thick Rogers RO3035 substrate with a dielectric constant of 3.5. The structure parameters for line width and length were calculated by using equations (1)–(5) which are subject to W/t ≥ 1[12].

$$Z_0 = \frac{87}{\sqrt{\varepsilon_{r+1.41}}} * \ln\left(\frac{5.98*t}{0.8*W+t}\right) \quad (1)$$

$$W = \frac{7.48*t}{e^{\frac{Z}{87}*\sqrt{\varepsilon_{r+1.41}}}} - 1.25*t \quad (2)$$

$$\varepsilon_e = \frac{\varepsilon_{r+1}}{2} + \frac{\varepsilon_{r-1}}{2\sqrt{1+\frac{12t}{W}}} \quad (3)$$

$$\lambda_e = \frac{3*10^8}{f_0\sqrt{\varepsilon_e}} \quad (4)$$

$$L = \lambda_e/4 \quad (5)$$

W is the input, output or section width, t is the substrate thickness, Z_o is the characteristic impedance of the microstrip transmission line, ε_r is the relative permittivity of the substrate, ε_e is the effective permittivity of the substrate, λ_e is the effective wavelength, fo is the centre frequency, which is 6.85 GHz for this design and L is the microstrip transmission line length.

Table I. Geometry parameters for The UWB 1-to-2 power divider

I	Z_i (Ω)	R_i (Ω)	W_i (mm)	L_i (mm)
Input (port 1)	50	-	1.381	6.656
1	90.52	96.1	0.851	6.768
2	70.71	94.3	1.079	6.714
3	55.24	527	1.298	6.671
Output (port 2&3)	50	-	1.381	6.656

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***Abstract*—This paper presents a design procedure for a physically small, equal phase and equal power, 1-to-4 ultra-wideband Wilkinson power divider is presented. Initially, a 1-to-2 divider was designed and optimized for the full 3.1 GHz to 10.6 GHz range. The 1-to-4 divider was realized using three 1 to 2 dividers, and further optimized for full band insertion loss, return loss, and isolation. The circuits were constructed using a 0.75mm thick Rogers RO3035 substrate, and experimentally validated.**

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3	55.24	527	1.298	6.671
Output (port 2&3)	50	-	1.381	6.656

The centre-line of the input and output ports, and sections, can be considered to be the equivalent microstrip length for simplifying the design. A 50% mitre was used for minimizing the high VSWR due to excess capacitance at the square corners caused by microstrip discontinuities [13].

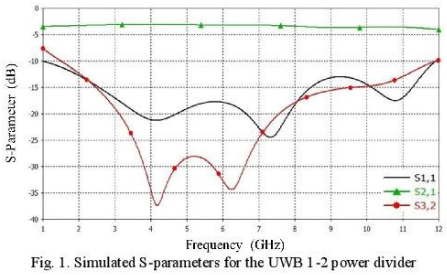

Fig. 1. Simulated S-parameters for the UWB 1-2 power divider

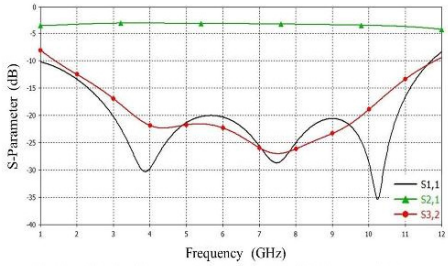

Fig. 2. Optimized S-parameters for the UWB 1-2 power divider

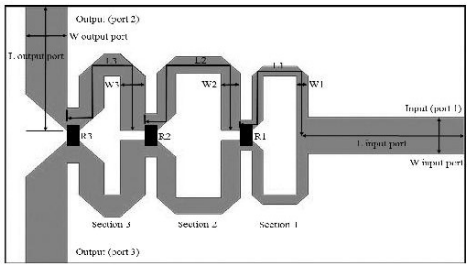

Fig. 3. Optimized layout for UWB 1-2 power divider

High dielectric constant materials have the ability to slow the wave propagation by reducing the signal wavelength, increasing the dielectric constant ensures lower wave speed at that particular frequency, but with a drawback of the narrower feed line as shown in (2) which will result in greater conductor losses. Also using high dielectric constant materials can produce higher couplings however, it can help to reduce radiation losses [14].

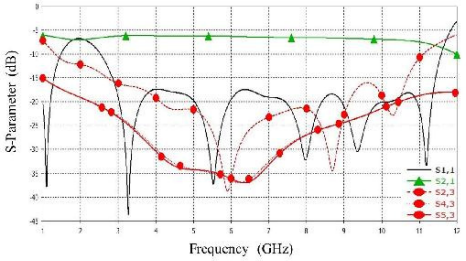

Fig. 4. Optimized S-parameters for the UWB 1-4 power divider

Generally, two types of materials are used for substrates, thermoset materials and PTFE. Thermoset materials are more affected by aging but it are more thermally stable. In addition PTFE is less effected by humidity[15].

Usually, two methods used in the industry for copper production which covers substrates. Electrode deposit copper (ED) and rolled copper. ED copper has a rougher surface, which means better boundary connection between the substrate and the copper but there will be greater conductor loss. While rolled copper has a smoother surface which helps to reduce the conductor loss, it achieves a weaker boundary connection with the substrate [14]. Rogers RO3035 substrate is a high-frequency ceramic filled PTFE board manufactured for use in microwave applications. It was selected for the following reasons. The low loss tangent of this material is 0.0015 which acts to mitigate the effect of substrate losses on the insertion loss. The dielectric constant was not so high to reduce coupling between output ports. Besides that, taking in consideration (2) and (4), in which the width of the microstrip is directly related to the substrate thickness and inversely to the substrate dielectric constant. This helped to have a sufficient line width and length to counter any minor imperfections in the fabrication [16]. Generally, this substrate has good electrical, mechanical and thermal stability.

III. FULLWAVE ANALSYIS AND OPTIMIZATION

A fullwave analysis of the power divider circuits was carried out using the CST Microwave Studio transient solver and optimization toolbox. Fig. 1 shows the simulated S-parameters for the 2-port splitter circuit; both the return loss and the isolation are below -12.5 dB and -14 dB respectively, and the insertion loss is between -3.2 and -3.8 dB across the required band. The particle swarm algorithm was used to refine the return loss and isolation performance by manipulating the section widths and lengths, ports and resistor values.

Table 2. Simulated parameters for different power dividers in previous work

Reference No	S11 (dB)	S21 (dB)	S32 (dB)	Size (mm x mm)
[3]	-14.72	>-3.52	-15.36	13 x 32
[4]	-11	>-3.5	-20	12.2 x 18.5
[5]	-12	>-3.5	-10	16 x 18
[6]	-13	>-3.5	-10	16 x 32
[7]	-15	>-3.5	-10	20 x 11.56
[17]	-10	>-3.5	-10	21 x 34
[18]	-17	>-3.5	-6	15.5 x 22
[19]	-11	>-3.5	-14	16 x 17
Presented work	-20	>-3	-17	12.6 x 19.6

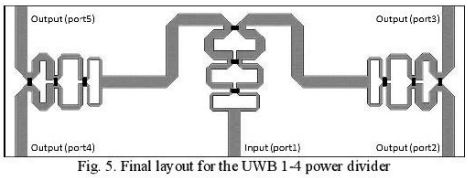

Fig. 5. Final layout for the UWB 1-4 power divider

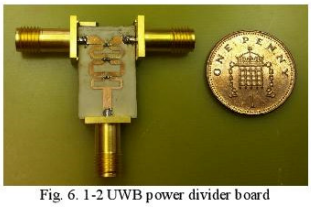
Fig. 6. 1-2 UWB power divider board

The optimized parameters are shown in Fig. 2, and the layout artwork for the 1-to-2 splitter is shown in Fig. 3, the board size was 12.42 mm × 19.56 mm. The optimized return loss and isolation show improvements of approximately 7.5 dB and 1.5 dB respectively, as can be seen from Figs. 2 and 3. The insertion loss appears to remain unchanged, this is essentially a function of the loss tangent and surface roughness [20], neither of which are not included in this optimization. The final model is the 1-to-4 splitter; optimized return loss and insertion loss values are shown in Fig. 4.

The final layout is shown in Fig. 5. The output of the first stage which are 50 Ω ports have been stretched to connect to the second stage. The impedance value remains unchanged as this depends on the thickness of the substrate and width of the microstrip, according to (2). There is a slight reduction in the return loss, which is recoverable by optimization. Fig. 4 shows a potential return loss below 20 dB for the full band of 1-to-4 splitter design, with board size of 60.16 mm × 19.94 mm. An insertion loss variation of between 6.2 dB and 7.2 dB is inferred, together with a port isolation below 16 dB, as shown in Fig.4

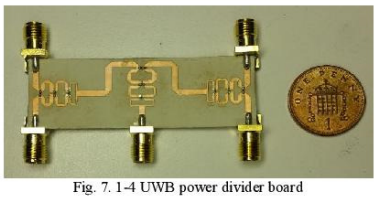
Fig. 7. 1-4 UWB power divider board

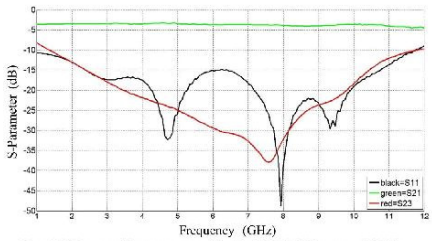

Fig. 8. Measured S-parameters for the UWB 1-2 power divider

A performance comparison was made between these designs, and several alternatives taken from the open literature, [3-7] and [17-19]. A summary is given in Table 2. The comparison was made on reported physical size, and return loss and isolation performance.

IV. PROTOTYPING AND MEASUREMENTS

Prototype circuits were fabricated n a 0.75 mm Rodgers RO3035 substrate. 100 Ω surface mount resistors were used on each of the first two sections, and a 432 Ω surface mount resistor was used on the third section. The resistor footprint was 1 mm × 0.5 mm, which allows a 0.5 mm gap between the two branches of the splitter. The 1-to-2 and 1-to-4 splitter variants are shown in Figures 6 and 7, and their scattering parameters are shown in Figures 8 and 9.

Both splitter responses show potentially useful realizable bandwidths for a return loss better than 15 dB. For the 1-to-2 splitter, the observed range is between 2.5 GHz and 10.5 GHz, giving a nominal bandwidth of 8 GHz. The corresponding range for the 1-to-4 is between 1 GHz and 11.5 GHz, giving a nominal bandwidth of 10.5 GHz. The realizable bandwidths for a 10 dB return loss are 10.5 GHz (i.e. between 1 GHz and 11.5 GHz) and 8.75 GHz (i.e. between 2.5 GHz and 11.25 GHz) for the 1-to-2 and 1-to-4 splitters respectively. The insertion losses (3 dB ±0.2 dB and 6 dB ±0.13 dB) were found to be consistent with the above bandwidths and for the simulated models.

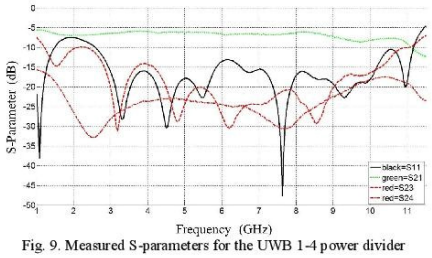

Fig. 9. Measured S-parameters for the UWB 1-4 power divider

V. CONCLUSION

The design of a physically small UWB 1-to-4 power divider has been discussed. A multi-section device was analysed and prototyped for full UWB operation over the range from 3.1 GHz to 10.6 GHz; the simulated and measured performances were in close agreement. These compact sized circuits should be particularly well-suited for use in UWB antenna array feed networks.

ACKNOWLEDGMENT

Ammar H. Ali would like to acknowledge support from the Higher Committee for Education Development in Iraq (HCED).

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A Design Procedure

for a 1-to-4 Ultra-Wideband Wilkinson Power Divider

By Ammar H. Ali, Professor Raed A. Abd-Alhameed, Yim Fun Hu, Mark B. Child and Costas Kyriacou

The design of a physically small, equal phase and equal power 1-to-4 ultra-wideband Wilkinson power divider is presented. Initially, a 1-to-2 divider was designed and optimised for the 3.1GHz-to-10.6GHz range. The 1-to-4 divider was then built using three 1-to-2 dividers and further optimised for full-band insertion loss, return loss and isolation. The circuits were constructed using a 0.75mm thick Rogers RO3035 substrate, and experimentally validated.

Introduction

Power dividers are important for impedance matching in many microwave and RF systems. In 1960, E.J. Wilkinson added an isolation resistor to a T-junction power divider, making a quarter-wave impedance transformer to enhance the return loss and isolation between outputs [1]. This design has the disadvantage of narrow operational frequency bandwidth.

Several methods have been adopted to increase the bandwidth such as the introduction of additional sections [2] or stabs to a section [3], combining these two previous methods [4] or using a slotted ground technique [5]. Since the commercial use of Ultra-Wideband (UWB) technology started in 2002 [6], a large number of papers have been published by researchers and industry especially for the 3.1-10.6GHz spectrum band. The UWB power divider must satisfy bandwidth requirement, constant insertion loss and a high degree of isolation between ports [7].

UWB power divider design

This article concerns the design and validation of a 1-to-4 power divider. The first step is to design a 1-to-2 power divider, afterwards combining three of them to make a two-stage 1-to-4 divider.

Generally, a single section Wilkinson power divider consists of two branches of 70.7Ω quarter-wave transformers terminated with a 100Ω resistive load. However, such power dividers have narrow bandwidths [8]. To increase this, additional sections of quarter wave transformers could be added and also terminated with resistive loads to increase output port isolation [9]. Examples of quarter-wave transformers and their resistive loads can be found in several tables and charts [9-11].

Initial section impedances and load values for the single-stage UWB power divider used in this work are shown in Table 1 opposite - the following equations allow the width and length of each section to be calculated [12]:

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Ammar received the B.Eng. degree in Electronic and Communication engineering from the University of Technology, Baghdad, Iraq in 2001 and M.Sc. in Communication Network Planning and Management from the University of Portsmouth, UK, in 2009. He has been a research student in the Antennas and Applied Electromagnetics research group within the Electronics, Communications and Information Systems Engineering (ECISE), University of Bradford since 2014. His research focuses on beam steering antenna design. He has worked in several telecommunication companies, which gave him practical experience besides his theoretical knowledge in the telecommunications field.

Professor Yim Fun Hu

Professor Yim Fun Hu is Professor of Wireless Communications Engineering at the University of Bradford since 2005. She is the Leader of the Communications and Networks Research Unit and the Head of the Future Ubiquitous Networks Research Group in the Faculty of Engineering and Informatics of the same university. Prof. Hu has received considerable funding support through participation in and contributions to many flagship projects funded by the EU, European Space Agency, UK research funding councils, Innovate UK and industry. Her major research is in mobile, wireless and satellite communication networks and applications in vehicular communications networks (aircraft and trains), Internet of Things and digital health. Prof. Hu has published over 100 papers in scientific journals and international conferences, and co-authored one book, edited two books and contributed to five book chapters. Prof. Hu is a Fellow of the Institute of Engineering and Technology and a Senior Member of the IEEE.

Costas Kyriacou

Costas Kyriacou graduated with an Honours degree in Electrical & Electronic Engineering from Leeds Beckett (Metropolitan) University in 1995. In 1979, he joined British Telecom and gained an in-depth knowledge of analogue and digital transmission equipment, which includes RF, Optical and various Multiplexing Systems. In January 1997 he joined Yorkshire Cable Communications, where he was responsible for the testing/evaluation of a variety of RF and Optical products and providing a support role for the network and the headend staff. Whilst at Telewest/Virgin Media, as CPE Hardware Development Manager and Engineer, his responsibilities were for all aspects of testing, test development, product/system evaluation and design with recommendations, laboratory manager and principle authority in the RF, Optical and CPE hardware discipline. This included a variety of hardware CPE, wireless gateway products and test developments. He now works for Thales as a hardware engineer.

Mark B. Child

Mark B. Child was born in Halifax, England, in 1967. He received a BSc (Hons) in Physics from Lancaster University in 1990 and an MSc in Radiation Physics from St. Andrew's University in 1994. From 1998 to 2007, he was a senior development engineer involved with BTS filters and antennas at Filtronic plc. From 2008 to 2015, he was a research engineer and part-time lecturer with the electromagnetics and antennas group at Bradford University. His research interests include electromagnetism and microwave engineering, with reference to the theory, design and computer modelling of filters and small antennas.

> **Power dividers are important for impedance matching in many microwave and RF systems.**

$$Z = \frac{87}{\sqrt{\varepsilon_{r+1.41}}} * \ln\left(\frac{5.98 * t}{0.8 * W + t}\right) \quad (1)$$

$$W = \frac{7.48 * t}{e^{\frac{Z}{87}} * \sqrt{\varepsilon_{r+1.41}}} - 1.25 * t \quad (2)$$

$$\varepsilon_e = \frac{\varepsilon_{r+1}}{2} + \frac{\varepsilon_{r-1}}{2\sqrt{1 + 12t/W}} \quad (3)$$

$$\lambda_e = \frac{3 * 10^8}{f_o\sqrt{\varepsilon_e}} \quad (4)$$

$$L = \frac{\lambda_e}{4} \quad (5)$$

where (Z) is the microstrip impedance, (ε_e) is the effective permittivity, (W) is the microstrip width, (t) substrate thickness, (L) is the microstrip length and (λ_e) is the effective wave length. (f_o) is the central frequency, equal to 6.85GHz. The centre line of ports and sections is taken to be the equivalent microstrip length to simplify design and a 50% mitering method is used to minimize the effect of reflections from microstrip bending [13].

I	Z(i) / Ω	R(i) / Ω	W(i) / mm	L(i) / mm
Input (port 1)	50	-	1.381	6.656
1	90.52	96.1	0.851	6.768
2	70.71	94.3	1.079	6.714
3	55.24	527	1.298	6.671
Output (ports 2 & 3)	50	-	1.381	6.656

Table 1: Geometry parameters for The UWB 1-to-2 power divider

The circuit was fabricated on a 0.75mm thick RO3035 substrate with permittivity (ε_r) of 3.5. This substrate is chosen in consideration of equation (2), showing that the line width is directly related to the substrate thickness and inversely related to the substrate permittivity. The resulting line width must be thick enough to comply with fabrication tolerance [14]. Additionally, this substrate has a low tangent loss of 0.0015, thus reducing insertion loss.

Simulation and optimisation

The simulation of the UWB power divider was performed using CST microwave studio 2015. Initially, the return loss was below 12.5dB, the isolation was less than 14dB and the insertion loss was between 3.2 and 3.8dB over the band. After optimising widths, resistor values and ports and section lengths, a better return loss and isolation were achieved (see the optimised S-parameter values in Fig. 1 below).

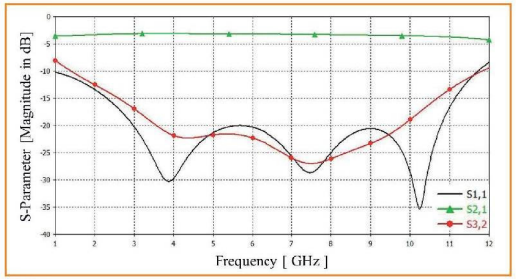

Figure 1:

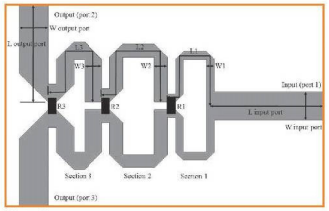

Figure 2:

The final layout for the 1-to-2 UWB power divider is shown in Fig. 2, with overall size of 12.52mm x 19.56mm. The proposed power divider is one of the smallest size power dividers in comparison with UWB power dividers from previous work, and with very good performance as shown in Table 2 [3, 4, 15-17].

After optimisation, the return loss improved by 7.5dB, with a 1.5dB minimum improvement for isolation over the band. The insertion loss did not change, as it is depends on the substrate tangent loss and metal surface roughness [18] which were not changed by the optimisation.

To construct the 1-to-4 power divider, three 1-to-2 power dividers were used. The final structure has been optimised for the best S-parameter values: optimised isolation, insertion and return loss are shown in Fig. 3 below.

The output ports of the first stage, with impedance 50Ω, have been stretched to connect to the second stage. The impedance value was unchanged, as it depends upon the microstrip width and substrate thickness as in Equation 2. There was a slight effect on reducing the return loss, subsequently corrected by optimisation.

Fig. 3 below shows that the achieved return loss is below 20dB over the band for this small 1-to-4 power divider structure (60.16mm x 19.94mm). The insertion loss is between 6.2 to 7.2dB, and the isolation between output ports is below 16dB over the UWB band.

Fabrication and measurements

To validate simulated results, the 1-to-4 power divider was fabricated as above on RO3035 substrate dielectric, of 0.75mm thickness, relative permittivity 3.5 and tangent loss of 0.0015. Surface-mounted resistors were 100Ω for the first and second sections and 432Ω for the third section. The resistors were

Reference No	S11	S21	S32	Size
[3]	>12dB	>3.5dB	>10dB	16mm x 18mm
[4]	>13dB	>3.5dB	>10dB	16mm x 32mm
[15]	>10dB	>3.5dB	>10dB	21mm x 34mm
[16]	>17dB	>3.5dB	>6dB	15.5mm x 22mm
[17]	>11dB	>3.5dB	>14dB	16mm x 17mm
Present work	>20dB	>3.5dB	>17dB	12.6mm x 19.6mm

Table 2. Simulated parameters for power dividers in this and previous work

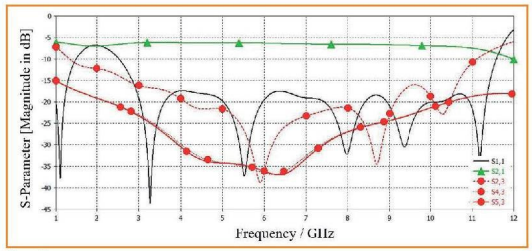

Figure 3:

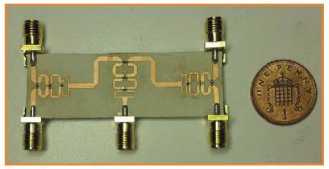

Figure 4:

0402 imperial size (1mm x 0.5mm) to ensure a 0.5mm gap between the two branches of the power divider. The fabricated power divider is shown in Fig. 4 above.

An Agilent N5242A network analyser was used to measure S-parameters for the 1-to-4 power divider, shown in Fig. 5. The return loss is below 13dB over the band, with isolation below 14dB, while the insertion loss is between 6dB and 8dB.

The experimental and simulated results largely agree. Small differences could be due to several reasons, such as resistor positioning and soldering. Experiments do show that the return loss changes when the resistors are shifted, and also that the amount of solder used with the connector affects the results. On top of that, fabrication tolerance also has its impact on results.

Conclusion

This article has presented a small size UWB 1-to-4 power divider. A multiple section method has been used to achieve UWB operation (3.1GHz-10.6GHz).

The small size designs for both 1-to-2 and 1-to-4 dividers make them suitable for applications where size and performance are critical, such as in antenna array applications. The simulation and experimental results largely agree, which validates the design approach.

Acknowledgments

This work was supported by the Higher Committee for Higher Education Development in Iraq (HCED) and the Yorkshire Innovation Fund, Research Development Project (RDP) Ref: RY0042 including the TSB grant application through Knowledge Transfer Programme KTP008734.

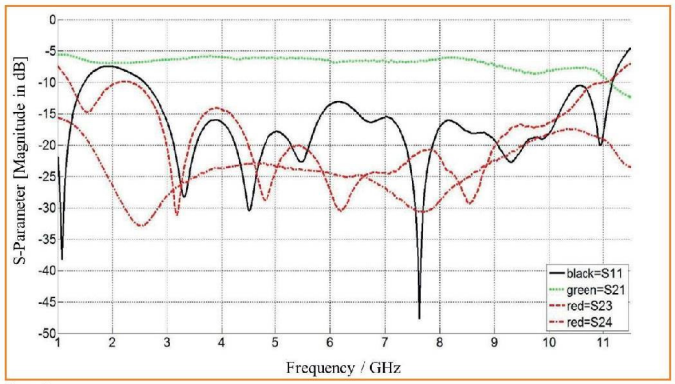

Figure 5:

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From the Archives

by Dr. Roger Blakeway

After 70 years of existence, the Society has accumulated a tremendous amount of information and data, not only about the Society itself but also about the industry in general. Of course, until the '90s most of this information was in paper form with the earliest material somewhat yellowing with age. Over the last 12 years I have scanned, OCR'd and edited all our CTE and Broadband Journals and made them available as downloadable PDF files.

The result is a complete archive of the Society's Journal from 1946 to date, all available to members as a download from the website at **http://www.thescte.eu/downloads**. Over the last few years, we have also provided an interactive page-turning version of each issue which is also available online. We intend to progressively make the complete archive available as page-turning versions.

On the website, you will also find some fascinating documents from 1945 showing how the Society was first set up together with copies of every Annual General Meeting up to the current day. We also have copies of 'Crosstalk' which was aimed at technicians and produced from 1998 to 2002.

Also available online is an interesting archive of CableVision News. This was originally published by the Cable Television Association (CTA) starting in 1973 and provides an interesting insight into cable at a business level before the introduction of the new cable franchises in 1983/4.

With such a valuable and fascinating collection of information from the past, we would encourage all our members to take a peek into the archives.

To give you a taste of what's on offer, we have decided to re-publish a selection of papers from the past. On the next page, you can read 'Passive Components for Cable Television Systems - Part 2' by Chris Swires and edited by Ray Seacombe, published in Vol.11 No.7 of CTE. We have tried to keep the original format and apologise that the resolution of some of the figures are not to our usual standard.

This provides an interesting 'compare and contrast' to the preceding article on the design of a modern Ultra-Wideband power divider.

Dr. Roger Blakeway
CEO, SCTE

A Novel Multi-standard Dual-Wide Band Polygon SLSIR Filter

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***Abstract*—A novel multi-standard dual-wide band filter with a compact size of only 8.8 mm by 16.8mm is designed and developed for transceiver devices. The proposed filter has a fundamental bandwidth of 1.6GHz with fractional bandwidth (FBW) of 29.7% centered at the 5.4GHz band, and second bandwidth of 300.0MHz with FBW of 3.6% centered at the 8.15GHz band. The basic dual-wide bandwidth is attributed to the interaction of the novel modified polygon pair and upper stub loaded stepped impedance resonator. Moreover, the added down stub loaded stepped impedance resonator (SLSIR) further enhances the pass band performance by widening the bandwidth and optimizing reflection coefficient performance considerably. To validate the proposed ideas, the multi-standard filter is designed and simulated by Ansoft HFSS software. The simulated results agree well with the theory predictions. The featured broad bandwidths over two frequency bands and the miniaturized size of the proposed filter make it very promising for applications in future multi-standard wireless communication.**

Keywords—Dual-wide band filter, multi-standard, stub loaded modified step impedance resonator, wireless communication.

I. INTRODUCTION

In recent years, wireless communication facilities such as wireless transceivers have been exerting an increasingly vital impact in the field of microwave and radio frequency communication. One of the most important modules in wireless communication system is the filter. Filters play a critical role in passing desired frequency bands and stopping the unwanted ones including noise signals. Therefore, performance of the filter greatly influences performance of the whole wireless communication system [1-9].

With the requirements in the current increasingly stringent frequency spectrum resources and the development of advanced multi-standard wireless communication systems, multi-standard filters have become a necessity for the state-of-the-art multifunction wireless transceivers for the mobile devices. Such filters are generally required to be capable of covering the frequency bands of IEEE 802.11a, IEEE 802.11h, IEEE 802.11j and IEEE 802.11n, all of which operate at 5 GHz bands; IEEE 802.11ac, which was approved by IEEE in January 2014 and provides very high throughput (VHT) wireless local area networks (WLANs) in the 5GHz band and IEEE 802.11p, which is intended for use in vehicular communication systems as well as specifies WLAN in the licensed Intelligent Transportation Systems (ITS) band of 5.9GHz (5.850-5.925GHz). Furthermore, ever increasing implementation of the communication between earth and space satellite further increases the Global Positioning System 'GPS' (at which the frequency bands centered at 5.75 GHz) requirement and X-band requirement such as International Telecommunication Union (ITU) designed earth-space satellite communication band (7.9-8.4GHz), transmission frequency bands of earth observation satellite systems including Terra (frequency bands centered at 8.2125 GHz), Aqua(frequency bands centered at 8.16GHz) and so on. Recently, many dual band filters have been designed to satisfy such stringent requirements [1-5]. However, most of them with a miniaturized size fail to cover the required frequency bands, especially at the lower frequency band due to the narrower dual bandwidth [1-3] or require a considerable filter size or thickness, which usually makes them difficult to integrate within mobile devices or portable wireless modules [1][4][5].

In this paper, we propose a novel multi-standard filter whose size is only 8.8mm×16.8mm. This filter is capable of generating two wide operating bands that effectively cover IEEE802.11a/802.11h/802.11j/802.11n/802.11ac (frequency bands cover 5GHz); IEEE 802.11p (frequency bands centered at 5.9 GHz); Global Positioning System (GPS) (frequency bands centered at 5.75 GHz); International Telecommunication Union (ITU) designed earth-space satellite communication band (7.9-8.4GHz) and most transmission frequency bands of earth observation satellite systems.

The proposed multi-standard filter's transmission zeros, which are used to realize the isolation of two pass bands as

well as the isolation between pass bands and out of band, are attributed to the mutual coupling of the modified polygon microstripe line. The in band performance of the proposed filter is mainly realized by upper shaped stub loaded stepped impedance resonator. This performances is further enhanced by adopting down shaped stub loaded stepped impedance resonator (SLSIR).Because there is no via hole or defect ground structure included in the filter structure, the structure is relatively simple and easily realized. The theory study of the multi-standard filter and configuration performance with simulation results are described in Section II, and the conclusion of this paper is given in Section III.

II. FILTER THEORY AND CONFIGURATION

A. The Introduction of The Novel Modified Polygon Pair

The configuration of the presented multi-band filter is illustrated in Fig. 1, in which the modified polygon pair forms a symmetric structure. Two modified polygons pair exert the effect of resonators which generate the basic curve of the filter second pass band and sufficient transmission zeros that are used to realize the isolation of two pass bands as well as isolation between pass bands and out of band. Further, two modified polygon resonators act as the function of feed lines for both upper and down shaped stub loaded stepped impedance resonators. Among them, the upper resonator mainly realizes dual-wide band, and the down resonator further enhances in band performances including widening bandwidth. In this work, the modified polygon resonator pair strips are fed by two 50Ω microstrip feed lines. The width (SW) and length (SL) of the 50Ω feed line is 0.6mm and 1.2mm, respectively.

B. The Shaped Stub Loaded Stepped Impedance Resonator

The shaped stub loaded stepped impedance resonators (SLSIR) of the proposed filter is shown in Fig. 2a. It is seemed that upper and down SLSIR couple with two polygon resonators in a folded line form and stepped-impedance stub is embedded in invagination part between two polygon resonators. This means saves much size of resonators and results in a more compact filter size without sacrificing filter performance. In order to simplify the analyses and calculation, SLSIR equivalent structure is derived, which is shown in Fig.2 (b). The equivalent structure includes a traditional SIR with the characteristic admittance Y_1, Y_2, and electrical length Θ_1, $2\Theta_2$, which is connected to a stepped-impedance stub in the middle. The stepped-impedance stub includes high impedance line with characteristic admittance $2Y_3$ and electrical length Θ_3, and low impedance line with characteristic admittance $2Y_4$ and electrical length Θ_4. Since SLSLR is symmetrical in structure, odd- and even-mode analysis is utilized.

For odd-mode excitation, the equivalent circuit is shown in Fig. 2c. According to the transmission line theory, the input admittance for odd-mode is expressed as:

$$Y_{in1}^{o} = -jY_2 \cot\theta_2 \qquad (1)$$

$$Y_{in,odd} = Y_1 \frac{Y_{in1}^{o} + jY_1 \tan\theta_1}{Y_1 + jY_{in1}^{o} \tan\theta_1} \qquad (2)$$

When $Y_{in,odd}=0$, equation(2) can be deduced as : $K_1\tan\Theta_1\tan\Theta_2=0$. Where $K_1=Y_1/Y_2$. Assume the electrical length ratio of the odd-mode resonance is: $\alpha_2=\Theta_1/(\Theta_1+\Theta_2)$. Then substitute this to (2), there is:

$$K_1\tan\Theta_2 - \cot\{\Theta_1(1-\alpha_2)/\alpha_2\}=0 \qquad (3)$$

The odd-mode solution of (3) is depend on K_1 and α_2.The ratio of the first two odd-mode resonance frequency can be determined by the length ratio α_2 and admittance ratio K_1 ,which are shown in Fig. 3.

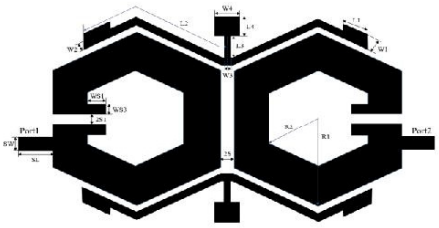
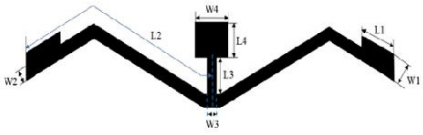
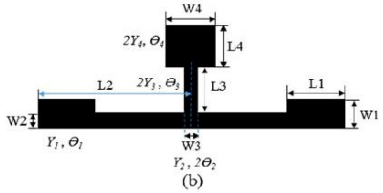


Fig1. The architecture of the proposed dual-wide band filter



(a)



(b)

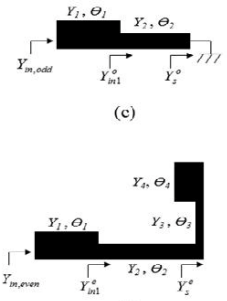


Fig 2. The modified SLSIR of the proposed filter and its equivalent structure

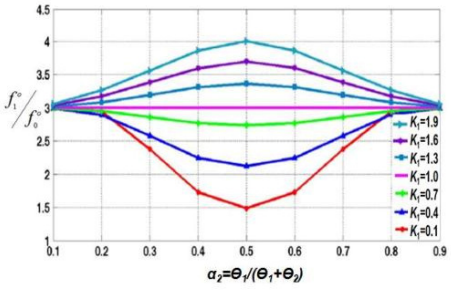


Fig. 3. Ratios of the first two odd-mode resonant frequency f_1^e/f_0^e under different electrical length ratio α_2 and admittance ratio K_4.

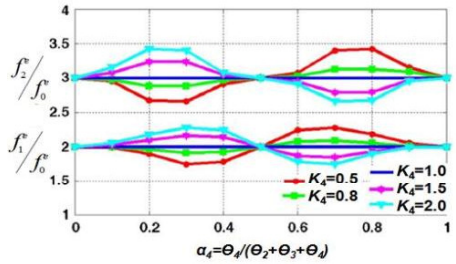


Fig. 4. Ratios of the first three even-mode resonant f_1/f_0^e, f_2^e/f_0^e under different electrical length ratio α_4 and admittance ratio K_4.

For even-mode excitation, the equivalent circuit is shown in Fig. 2d. The even-mode input admittance is expressed as:

$$Y_{in,even} = Y_1 \frac{Y^e_{in1} + jY_1 \tan\theta_1}{Y_1 + jY^e_{in1} \tan\theta_1} \quad (4)$$

In which $Y^e_{in1} = Y_2 \left(Y^e_s + jY_2 \tan\theta_2\right)/\left(Y_2 + jY^e_s \tan\theta_2\right)$,

$Y^e_s = Y_3 \left(jY_4 \tan\theta_4 + jY_3 \tan\theta_3\right)/\left(Y_3 + j(jY_4 \tan\theta_4)\tan\theta_3\right)$.

When $Y_{in,even}$=0, equation(4) can be deduced as : $K_4 \tan\theta_4 = \left[\tan(\theta_2+\theta_3) + K_1 \tan\theta_1\right]/\left(K_1 \tan\theta_1 \tan(\theta_2+\theta_3) - 1\right)$, in which $K_4=Y_4/Y_3$. The relationship among three even-modes, different electrical length ratio α_4 and admittance ratio K_4 is shown in Fig. 4. When $Y_1=Y_2=Y_3$ is supposed for simplicity, we can get $Y_{in,odd} = -jY_2 \cot\theta_2$ and Θ_2=90° when $Y_{in,odd}$=0. The fundamental odd-mode resonance frequency is:

$$f_0 = c/\left(4L_2\sqrt{\varepsilon_{eff}}\right) \quad (5)$$

The input admittance for even-mode resonance frequency is express as:

$$Y_{in,even} = jY_3 \frac{Y_4 \tan\theta_4 + Y_3 \tan(\theta_2+\theta_3)}{Y_3 - Y_4 \tan\theta_4 \tan(\theta_2+\theta_3)} \quad (6)$$

When $Y_{in,even}$=0, $K_4 \tan\theta_4 + \tan(\theta_2+\theta_3) = 0$ and further $K_4 \tan\alpha_4\theta_T + \tan(1-\alpha_4)\theta_T = 0$.

In this case, the stub loaded stepped impedance resonator generates one odd-mode frequency and two even-mode frequency. A thing that needs to be mentioned is because of irregular shape of the feed line(including polygon pair) to SLSIRs and the influence of coupling between two polygon resonators, even-mode frequency of SLSIRs can be tuned by combining theory values and empirical values to make it locate into desired frequency bands.

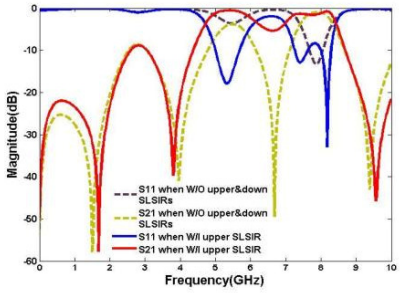


Fig. 5. The magnitude response S11 and S21when there is only polygon pair and when polygon pair coupled with upper SLSIR

C. *The superimposition of Polygon Pair Waveform and Stub Loaded Stub Impedance Resonator Waveform and The Isolation between Bands*

Because the modified polygon pair provides the basic curve of the filter second pass band and four transmission zeros including the third transmission zero of 6.68GHz, which is shown in dash lines in Fig. 5. Using this feature, we design the upper stub loaded stepped impedance resonator's odd-mode

frequency which is also SLSIR's fundamental frequency to be located at 5.3GHz.According to equation (5), we get the length $2L_2$ is equal to $\lambda_g/2$ (a half of wavelength of SLSIR) and the value of L_2 is 4.4mm when f_0 is 5.3GHz. Then external and internal radius of the polygon is set as R1=4.1 and R2=2.8mm, respectively. The two even-modes frequencies are tuned by changing the dimension of stepped impedance stub W_3, L_3, W_4 and L_4 in order to make it locate in 5-6GHz band and X-band. In this work, we set W_3=0.2mm, L_3=0.3mm, W_4=0.4mm and L_4=0.1mm. The electrical length of L_2, L_3 and L_4 is 90.0°, 6.1°and 2.0, respectively. From solid lines shown in Fig. 5, we know that after adopting the upper SLSIR, dual wide bands including 5.0-5.7GHz centered at 5.34GHz with fractional bandwidth (FBW) of 13.0% and 8.0-8.3GHz centered at 8.14GHz with FBW of 3.7% are realized with the help of polygon pair.

The magnitude response S11 and S21 of two occasions is shown in Fig. 6. The first occasion is when only the modified polygon pair with upper stub loaded stepped impedance resonator play roles, which is shown as dash lines. The second occasion is when modified polygon pair, upper and down stub loaded stepped impedance resonator play roles, which is shown as solid lines. It is seem that by adopting down stub loaded stepped impedance resonator, first pass band performance including bandwidth performance and reflection loss performance is improved considerably. The first pass band bandwidth of the proposed filter is broadened to 4.6-6.2GHz centered at 5.4GHz with fractional bandwidth (FBW) of 29.7% and second pass band bandwidth is 8.0-8.3GHz centered at 8.15GHz with FBW of 3.6% with the interaction of down SLSIR, upper SLSIR and modified polygon pair.

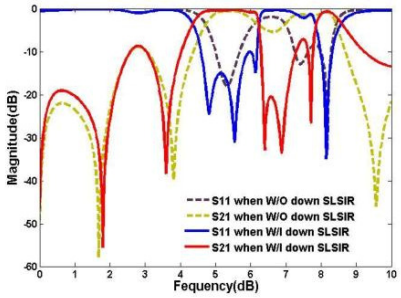


Fig. 6. The magnitude response S11 and S21 when polygon pair coupled with upper SLSIR and when polygon pair coupled with upper and down SLSIR

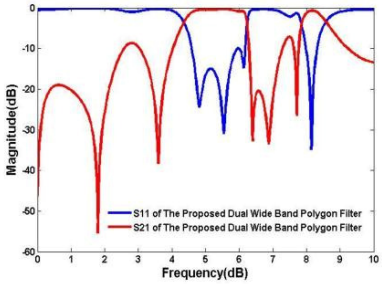


Fig. 7. The final results of the proposed dual-wide band filter

The final results of the proposed dual-band filter is shown in Fig.6.The substrate adopted in this work is Rogers RO3010 whose dielectric constant is 10.2 and thickness is 0.635mm.In the model, six transmission zeroes 0GHz, 1.80GHz, 3.60GHz, 6.40GHz,6.88GHz and 7.72GHz are generated. These transmission zeroes provides well isolation between desired dual bands, suppression of out of band interruption and enhancement of the frequency selectivity. The gap width between two resonator pair is 2S=0.2mm and another gap width 2S1=0.2mm.

III.CONCLUSION

A novel multi-standard dual-wide band filter with a compact size is designed and developed for wireless communication system such as mobile devices.This proposed filter covers a fundamental bandwidth of 1.6GHz with fractional bandwidth (FBW) of 29.7% centered at the 5.4GHz band and second bandwidth of 300.0MHz with FBW of 3.6% centered at the 8.15GHz, while occupy a miniature area of only 8.8mm by 16.8mm. By utilising novel modified polygon pair and upper stub loaded stepped impedance resonator, dual bands and sufficient transmission zeroes are generated. The added down stub loaded stepped impedance resonator further enhances the first pass band performance by widening the bandwidth and optimizing reflection loss performance considerably. What's more,the folded and embedded structure of two SLSIRs saves much size of the proposed filter compared to previous SLSIRs without sacrificing filter performance. The multi-standard filter is designed, described and fully simulated. The Ansoft HFSS software simulated results agree well with the theory predictions. The featured broad bandwidths over dual applicable frequency bands and the miniaturized size of the proposed filter make it very promising for applications in future multi-standard wireless communication.

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Design of a Sierpinski Patch Antenna around 2.4 GHz/5GHz for WiFi (IEEE 802.11n) Applications

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Abstract—In this paper, a low-cost dual-band printed antenna that employs Sierpinski fractal geometry is proposed for possible integration to IEEE 802.11n WLAN standards access points. The designed antenna covers two wireless spectrum bandwidth, they are the ISM 2.4 GHz and the U-NII 5 GHZ. The antenna geometry is confined within a compact size of 75 × 75 × 1.8 mm³. The antenna is mounted on partial ground and fed by microstrip line. It is modelled and optimized using the well-known CST software and the results in terms of reflection coefficient, VSWR, Bandwidth and power Gain are illustrated and compared to previous published literatures.

Keywords—Sierpinski; Fractal; Antennas, IEEE 802.11n, ISM band; Power Gain.

I. INTRODUCTION

One of the important objectives in radio communication systems is the design of wideband, or even multiband, small antennas with low profile for employment in commercial communications systems. Fractal antenna has been attest to be an useful technique to design small and multiband antennas, and display space filling properties that can be exploited to miniaturize standard antenna elements, like as dipoles and patches [1-2], and overcome some of the limitations of small antennas. Some solutions of this limitation is that fractal antennas are compacted in small space, and exhibit input resistances that are much greater than the classic geometries of dipoles , loops or patches.

In this paper, a printed antenna that employs Sierpinski fractal geometry is proposed foir possible integration to IEEE 802.11 n access points standards. The antenna covers dual band with acceptable radiation performance. First resonance frequency centered at 2.467 GHz while the second at 5.347 GHz.

II. THE 802.11N NORM

802.11n standard offer several advantages over previous wireless LAN technologies. The most notable advantages are essentially improved reliability and greater application data throughput. 802.11n act in both the 2.4 GHz and 5 GHz bands, acheiving the compatibility with pre-existing 802.11a/b/g deployments.

Wireless solutions depend on the 802.11n standard use various techniques to improve the reliability, throughput, and predictability of wireless LANs. The three primary addition are:

- Multiple Input Multiple Output "MIMO" technology
- Channel link (40MHz Channels)
- Packet aggregation

Together, these techniques permit 802.11n solutions to achieve an approximate fivefold performance increase over current 802.11a/b/g networks.

Devices with MIMO technology are characterized by the number of transmit (M) and receive (N) antennas they use simultaneously, a 2x1 MIMO AP transmits through two antennas and receives through one antenna[8], while a 3x3 MIMO AP transmits and receives through three antennas. Indeed, three transmit antennas generally provide more bandwidth than two transmit antennas [3].

III. ANTENNA STRUCTURE

This fractal geometry constructed by scaling the initial triangle (Fig 1-a) by one half (the generator). Application of the generator for the first time leaves three smaller filled triangles, the result is shown in (Fig 1-b), to which we may apply the scaled copy of the generator again. The corresponding structure is shown in (Fig 1-c). We iterate this process one more step to obtain (Fig 1-d), and so on [1-2].

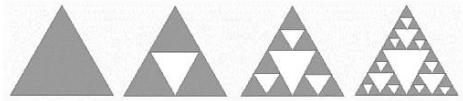
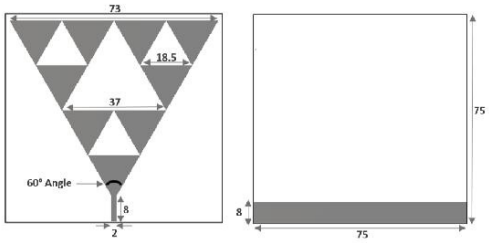


Fig 1: a) Initial triangle b) 1st Iteration c) 2nd Iteration d) 3rd Iteration

The configuration of proposed antenna is shown in (Fig 2). The second iteration of the Sierpinski geometry is considered. The radiating element is a Sierpinski equilateral triangle printed on a 1.8 mm thick substrate with dimensions (75 × 75) mm^2 and dielectric constant εr=2.5. It is fed by microstrip line with the size of (2 × 8) mm^2, and has a partial ground plane with area of (8 ×75) mm^2.



a) The front side view b) The back side view

Fig 2: Overview both side of the Sierpinski antenna

IV. Simulation Results and Analysis

In order to assess the effectiveness and reliability of the design, analysis is carried out and some representative results are presentd in the following to provide an overview of the performance. All the simulated data have been acquired by means of CST Microwave Studio.

A. Return loss, bandwidth and VSWR

The response of the return loss is shown in Figure 3. It can be noticed that the Sierpinski antenna is indeed resonating at 2.467 GHz and 5.347 GHZ with a return loss of 25.378 dB and 42.854 dB respectively.

The antenna also exhibits two frequency bands that cover widely the ISM and U-NII spectrums for IEEE 802.11n standard. The 10 dB bandwidth (i.e., at |S11| below -10 dB) is achieved at first resonant frequency centered at 2.467 GHz and wrap all the fourteen channel of ISM band, in addition, the second bandwidth appears at second resonant frequency centered at 5.347 GHz that in fact includes extensively the frequency range of 4.3-6.2 GHz. Indeed, the fractional bandwidth presented in (Table 1) of both operation frequencies is greater than 20 %, that it demonstrates a wideband antenna characteristics [5].

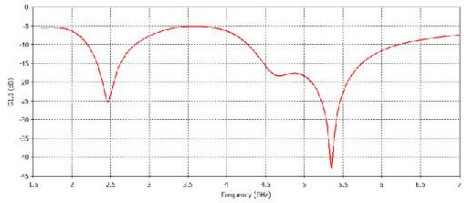


Fig 3: The simulated return loss for the proposed antenna

The input impedance of this antenna design is found extremely sensitive to the width of the microstrip feed line (Fig. 4) and thus the matching requirements at these frequencies are also fulfilled as indicated by the simulated results of return loss [4].

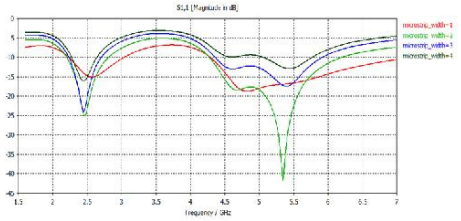


Fig 4 : return loss for different feed line width

The parameter VSWR for Voltage Standing Wave Ratio is a quantity that imply how well the impedance of antenna has matched, which describes the power reflected from the antenna, it is seen in (Fig 5) that VSWR for the two operational frequencies is a real and positive number and nearly to 1 (Table 1), where VSWR = 1 implies a matched load.

TABLE 1: MAIN PARAMETERS OF THE SIMULATED SIERPINSKI ANTENNA

Band	f_c (GHz)	Bandwidth		Return loss(dB)	VSWR
		(MHz)	(%)		
ISM	2.467	614.56	24.88	-25.378	1.1129
U-NII	5.347	1941.1	36.55	-42.854	1.0145

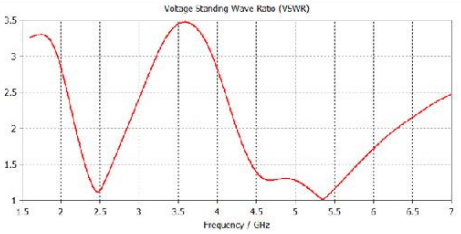
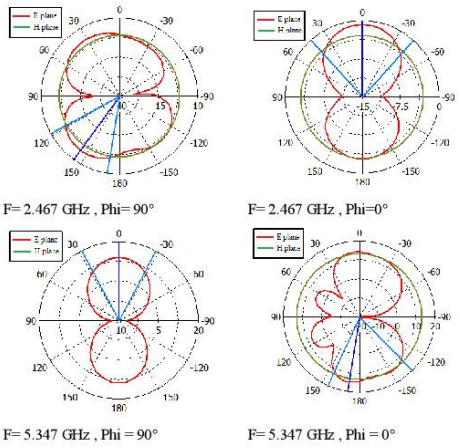


Fig 5: Voltage Standing Wave ratio Vs Frequency

B. Radiation pattern

The radiation pattern is determined in the farfield region and it is shown in (Fig 6) ,for both frequencies width two angles Phi = 0 and Phi = 90, the radiation patter is quite similar to a monopole antenna, it is omnidirectional for the first resonant frequency, in the second resonant frequency, two small beams appear and radiation pattern is quasi-omnidirectional [4].



F= 2.467 GHz , Phi= 90° F= 2.467 GHz , Phi=0°

F= 5.347 GHz , Phi = 90° F= 5.347 GHz , Phi = 0°

Fig 6: E and H plane radiation pattern of Sierpinski antenna at 2.467 GHz and 5.347 GHz.

V. Comparison of Fractal Sierpinski measured parameters width two commercial types of antenna.

In this section, the simulated results of various parameter of three Sierpinski antennas in a row shown in Figure 7 are given and compared with two types of commercial antennas as in Table 2.

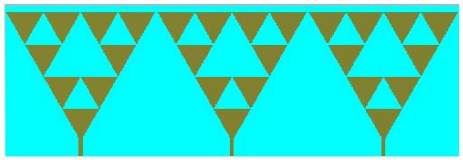


Fig 7: Overview of the three Sierpinski antenna

The first one [7] is a dual band 2.4 and 5 GHz patch antenna, was designed to operate with 802.11n MIMO access points, this antenna encloses three integrated 2.4 GHz patch antennas and three integrated 5 GHz patch antennas in one enclosure. The second antenna in [8] is a single band attained to MIMO wireless devices as 802.11n access points and using three dipole antennas.

As presented in Table 2, many advantages of the Sierpinski antenna is that the large bandwidth achieved for both bands that will significantly improve the data transmission compared to others published data.

Table 2: Comparison among Sierpinski simulated antenna Vs commercial patch and dipole antenna.

	Sierpinski antenna 3 x 3		MIMO Patch antenna 3 x 3 [7]		Dipole antenna 3 x 3 [6]	
Bands	**ISM**	**U-NII**	**ISM**	**U-NII**	**ISM**	**U-NII**
Frequency range (MHz)	2050-2726	4130-6245	2400-2500	5100-5850	2400-2485	-
Bandwidth (MHz)	675	2115	100	750	85	-
Gain	6.2 dBi	7 dBi	6 dBi	6 dBi	5 dBi	-
VSWR	1.11	1.0145	≤ 1.5	≤ 2.0	-	-
Dimension (LxWxH)	8.86 x 2.95 x 0.07 in		17.5 x 6.1 x 1.0 in		11 x 3.86 x 1.1 in	

The gain achieved is around 6.21 dBi for the ISM band and 7 dBi for the U-NII band, imply that the antenna has the ability to cover radio frequency energy further than patch and dipole as described in Table 2. It is also observed that the dimensions of three Sierpinski antennas are lower than the other types, that it will be easily added seamlessly to access point.

VI. Conclusion

A second iteration of Sierpinski antenna has been presented in order to cover ISM and U-NII bands for possible integration to IEEE 802.11n applications. The proposed antenna was compared with other published data and has shown a good promising radiation performances in terms the bandwidth and power gain. One can deduce that the proposed antenna could be recommended as possible candidate for IEEE 802.11n standards.

Acknowledgement

This work is carried out under the grant of the Fundacão para a Ciência e a Tecnologia (FCT - Portugal), with the reference number: SFRH / BPD / 95110 / 2013.

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A Novel Beam Steering Design for Phased Array Antennas

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Steerable Phased Array Antennas (PAAs) can be defined as multiple stationary antenna elements that are controlled by phase shifters. The PAA radiation pattern is steered electronically giving useful features in many applications. Thus, PAAs can replace the traditional mechanical rotation radars. There are a wide range of communication application which use steerable PAAs such as military radar systems, weather surveillance radars, and late generations of cellular systems, this is due to the significant performance that they provide compared with traditional mechanical radars, such as high scanning speed [1-5]. This Paper presents a novel, low-cost, compact size beam steering PAA which is based on a novel approach of integrating a low-cost, high performance phased shifters with their controlling boards within an antenna structure. Consequently, the system has been reduced to a compact structure for the antenna array and phase shifters, rather than the sophisticated PAA with two separate boards which are connected by RF coaxial cables. The proposed idea has been achieved by the following stages. Firstly, the steering vector weights matrix were calculated by Matlab. Then, four element uniform linear Microstrip patch antenna array with their feeding network power divider were designed and simulated using CST package. The RF-PCB for the 4-bit phase shifters were integrated within the antenna panel as shown in Fig 1 and Fig 2. The simulated results using Matlab and CST Software against measurements were presented. The practical results were quite reasonable and match the computed one as shown in Figs. 3 and 4, and they prove the success of the proposed system with high steering accuracy. The result presents a compact PAA system, working at a resonant frequency of (2.4 GHz), with (120^0) steering capability.

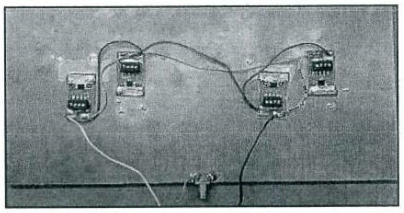

Fig.1: PAA Design Back Panel

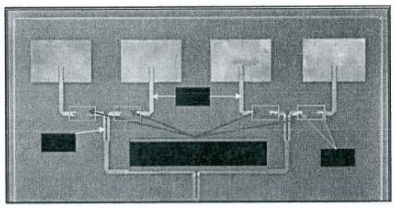

Fig.2: PAA Design Front Panel

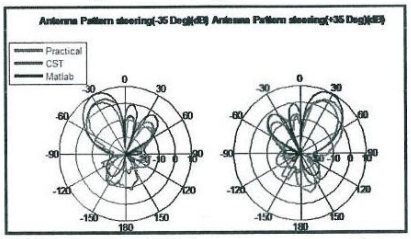

Fig.3: Scanning of (-35^0) Left Figure, ($+35^0$) Right Figure Matlab,CST and Practical

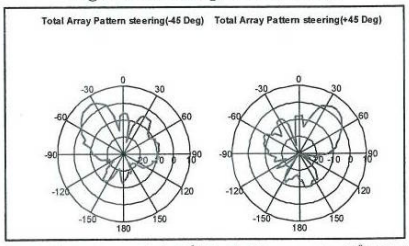

Fig.4: Scanning of (-45^0) Left Figure, ($+45^0$) Right Figure, XZ Plane, Practical

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Miniature 1 to 2 Ultra-Wide Band Power Divider

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The power divider considered as an important component in different telecommunication systems such as antenna arrays, mixers, phase shifters, modulators and demodulators [1]. Power dividers got a creative modification by E.J. Wilkinson in 1960 where an isolation resistor have been added to two half wave transformers to enhance the return loss and isolation between outputs. The problem of his design was that the power divider had a narrow bandwidth. To increase the operating bandwidth, several methods can be adopted such as adding additional sections for the power divider [2], adding stabs to the sections [3], combined the previous methods together [4] or using a slotted ground pane technique [5].

This work present the design of a miniature 1 to 2 power divider with a return loss below -20dB over a wide operating band between 3.1 and 10.6GHz that could be applied for several applications require small size, light weight and high efficient components. The layout of the power divider is shown in Fig.1 that has been designed and optimized using CST 2015 and then fabricated on RO3035 substrate dielectric with relative permittivity of 3.5 and thickness of 0.75mm. It was shown the power divider satisfied the bandwidth requirement, with constant insertion loss including higher isolation between the two output ports as depicted in Fig. 2. The return lose was achieved below -20 dB, the insertion loss between -3.2 and -3.5 with isolation below -15dB across the whole bandwidth spectrum. The overall design size was found small and compact with minimum rectangular size of 12.52mm x 19.56mm compared to several published works as in [1, 3, 4, 7, 8]. This power divider can be considered one of the smallest size very high operational performance.

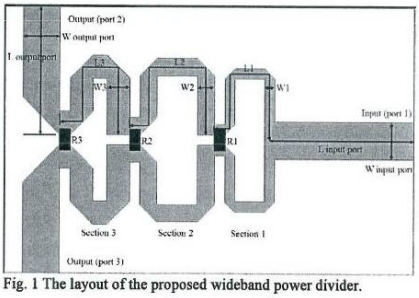

Fig. 1 The layout of the proposed wideband power divider.

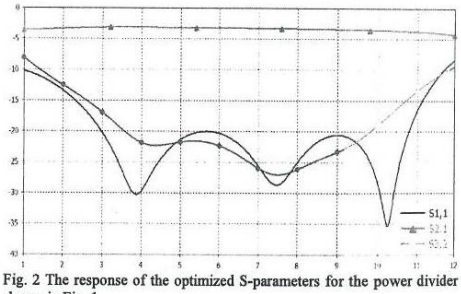

Fig. 2 The response of the optimized S-parameters for the power divider shown in Fig. 1.

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Design and Optimisation of Quadrifilar Helical Antenna for RFID Applications Using Genetic Algorithms

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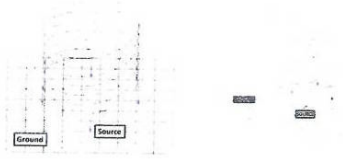
Antennas constitute a very important part of Radio Frequency Identification (RFID) systems. Coming in various forms and types, they are usually designed and intended to ensure maximum effective and efficient communication links between tags or transponders and their associated readers or interrogators. One of the primary challenges in the design and development of antennas in RFID applications as it is in other wireless applications is having an antenna with optimised parametric features that are desirable and in consonance with laid down specifications and functional requirements. These parametric features include but are not limited to: profile, gain, directivity, bandwidth and polarisation.

Radio Frequency Identification (RFID) systems which connote the physical interaction between a tag and a reader for automatic identification operate within the global bandwidth of (860 – 960)MHz as specified by the International Standards Organisation (ISO). RFID systems function by adopting a non-contact application of radio-frequency that does not require a line-of-sight channels. In order to optimise an RFID system, the orientation of the tags and associated readers must be fully established through the polarisation characteristics of their corresponding antennas. RFID tags are often designed to have linearly polarised dipoles. Consequently, their orientation in a typical RFID system is not always predictable.

The quadrifilar helical antenna (QHA) has been identified by previous works as a suitable antenna for tag reading in RFID and other wireless applications, due to its ability to give circular polarisation over a wide angular area [1-2]. Another excellent property of QHAs in terms of the symmetry of their geometry is their ability to give a cardioid-shaped radiation pattern regardless of the axial length and diameter. It has also been established that the inherent cardioid-shaped radiation patterns of QHAs can be made conical by extending the resonant fractional turns of the QHA to an integral number for improved characteristics [2]. Consequent to the aforementioned, a novel compact QHA was designed and optimised over a perfect ground to function optimally within the RFID global bandwidth of (860 - 960) MHz. The novel QHA antenna is named linearly-shifted quadrifilar helical antenna (LSQHA) because its elements are linearly-shifted and made compact as revealed in Fig. 1b. With reference to its helical elements and as can be observed, the proposed LSQHA design does not take the form of the conventional QHA. Specifying a finite ground and feeding of the LSQHA via an integrated feed network is proposed, to avoid the intricacy and losses associated with multiple feed points of a centre feed. At the risk of repetition, the novel antenna structure is achieved by linearly-shifting the helical elements of the conventional QHA by 90° using a defined phase quadrature distance. This design is expected to reduce the axial length and overall volumetric equivalent of the LSQHA, while retaining good axial ratio, high power gain and wide beamwidth coverage.



a b

Fig. 1: Antenna configurations examined: (a) QHA; (b) LSQHA

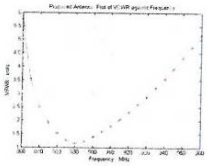


Fig. 2: Computed VSWR for the proposed LSQHA

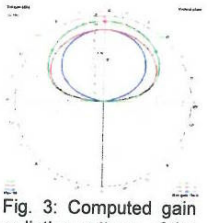


Fig. 3: Computed gain radiation patterns of the proposed antenna for one vertical cut plane.

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